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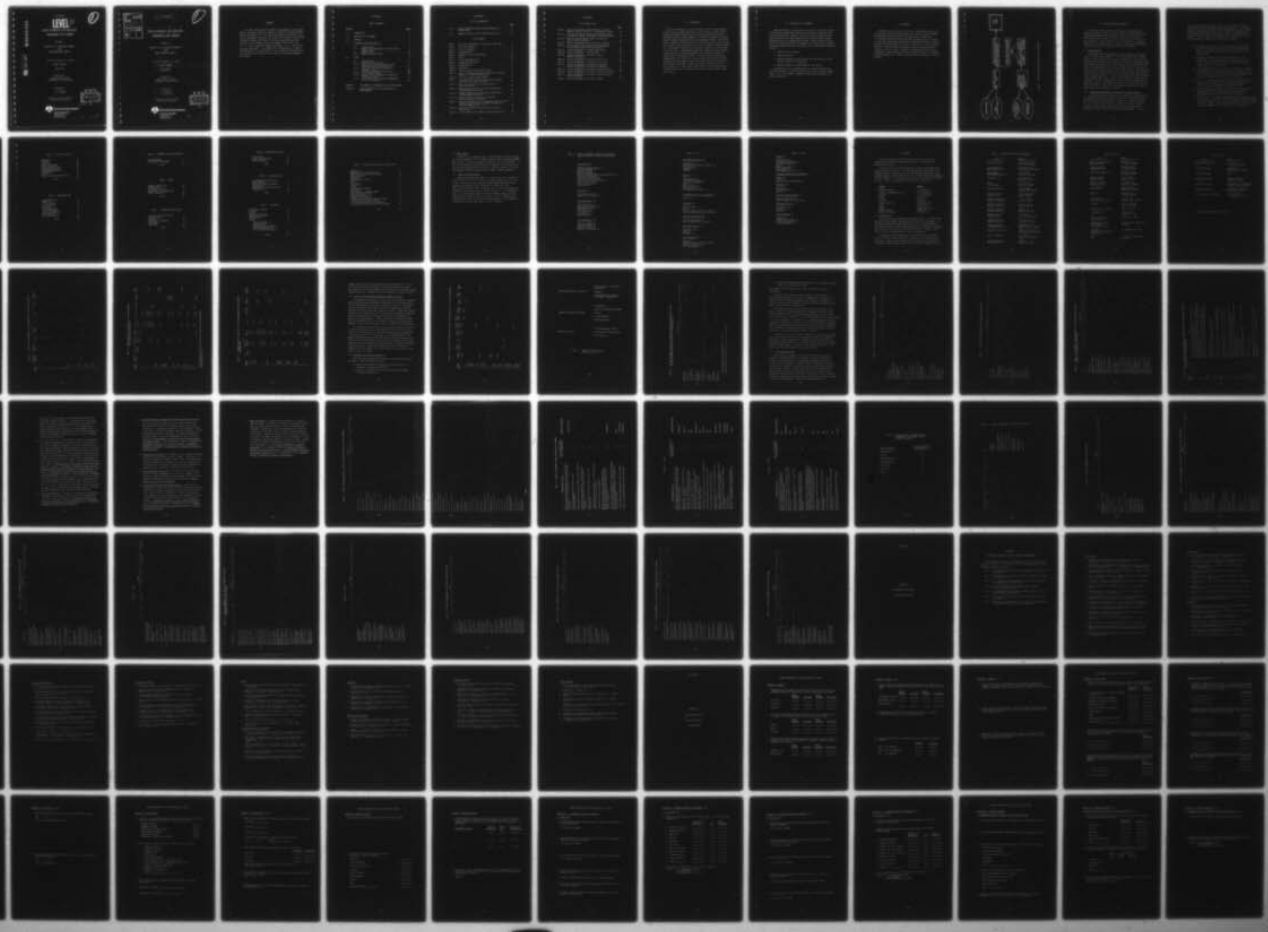

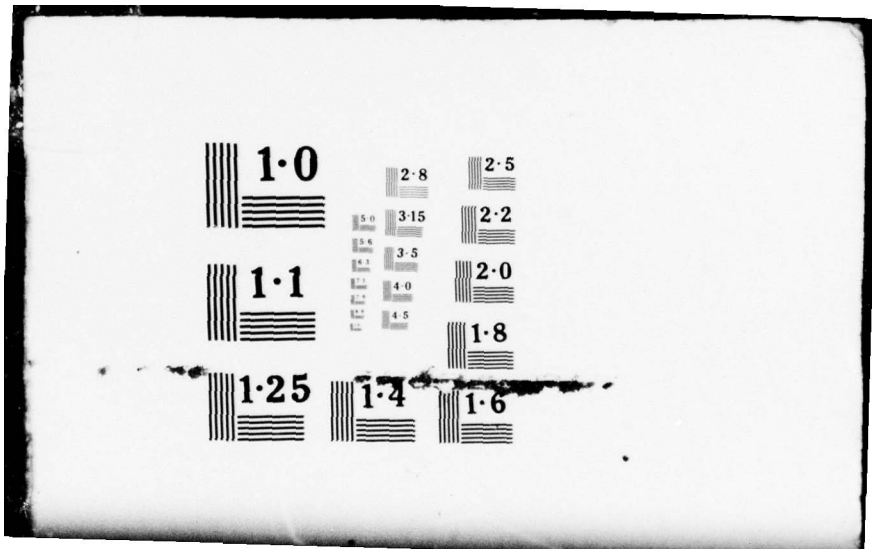
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LEVEL III

HYBRID TECHNOLOGY COST REDUCTION IMPROVEMENT STUDY PROGRAM

VOLUME I

RESULTS OF LITERATURE SEARCH
AND
QUESTIONNAIRE SURVEY

Contract N00163-77-C-0299

FINAL REPORT

APRIL 1978

Prepared for:

NAVAL AVIONICS CENTER
Indianapolis, Indiana 46218

Prepared by:

J. J. Licari
K. L. Perkins

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FOREWORD

This report describes work performed from September 2, 1977 through March 2, 1978 under Contract No. N00163-77-C-0299 for the Naval Avionics Center, Indianapolis, IN. This report was prepared by the Special Microcircuits Department, Electronic Devices Division of Rockwell International Corporation, Anaheim, California. The work was performed under the direction of M. W. McMurran, Director of Special Microcircuits, and Dr. J. J. Licari, Manager of Advanced Technology. Dr. K. L. Perkins was Principal Investigator. The authors wish to acknowledge Mr. M. Cowart, Program Manager for the Navy and Mr. S. Hart, Manager of Microelectronics for the Naval Avionics Center for their advice and guidance throughout the program.

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1.0 INTRODUCTION

Hybrid microelectronic circuits continue to fulfill a growing need in military avionics systems where physical size (volume and weight) and performance requirements cannot be met by the more conventional packaging techniques such as discrete components on printed wiring boards, and where cost and schedules preclude the use of more advanced methods. The military market is generally characterized as fast turnaround, high reliability, and low to medium volume for any one circuit type. A system is usually composed of a large number of diverse circuit types with usage of only 100 to 2000 circuits per year. These moderate quantities, coupled with lower nonrecurring design cost and shorter development times, often make hybrids an economic choice over custom LSI/VLSI. The hybrid market is dynamic and growing making it difficult to arrive at an annual sales figure; further most major aerospace companies have captive hybrid microcircuit facilities serving their system needs. However, estimates of the total military hybrid market for FY 1978, based on data received from the questionnaire, is $250 to $300 million, assuming an average price range of $250 to $300 per circuit.

2.0 OBJECTIVE OF THE PROGRAM

Though the benefits of using hybrid microcircuits in military avionics systems are well established, high cost and occasional reliability difficulties have been major concerns. The cost of the most complex military hybrid microcircuits has been reported to be as high as $3,000, though a representative price is between $200 and $300. More so than cost, reliability is of concern because of the complexity and wide variety of materials and processes that can be used and are being used. Opportunities therefore exist to:

a. reduce the cost of hybrids

b. improve reliability

c. provide guidelines and specifications for the qualification and control of materials and processes

d. provide a measure of standardization of end item use

The objectives of this program were first to define the major cost drivers and sources of reliability problems, and second to define programs that will be in the interest of NAVAIR to reduce costs, and assess and improve reliability.

3.0 APPROACH

Information on cost factors, reliability, unique problems associated with hybrid microcircuits, and technical areas requiring further research and development were retrieved from two main sources. These were: (1) The open literature including conference proceedings; and (2) contacts via a written questionnaire; telecons with selected individuals in industry, government and universities; and finally on-site visits. A chart of these sources of information showing the general sequence of steps that were followed is given in Figure 1. Based on an assessment of these data and a knowledge of hybrid technology programs already performed or in progress, program recommendations in various technology areas were made and priorities assigned.

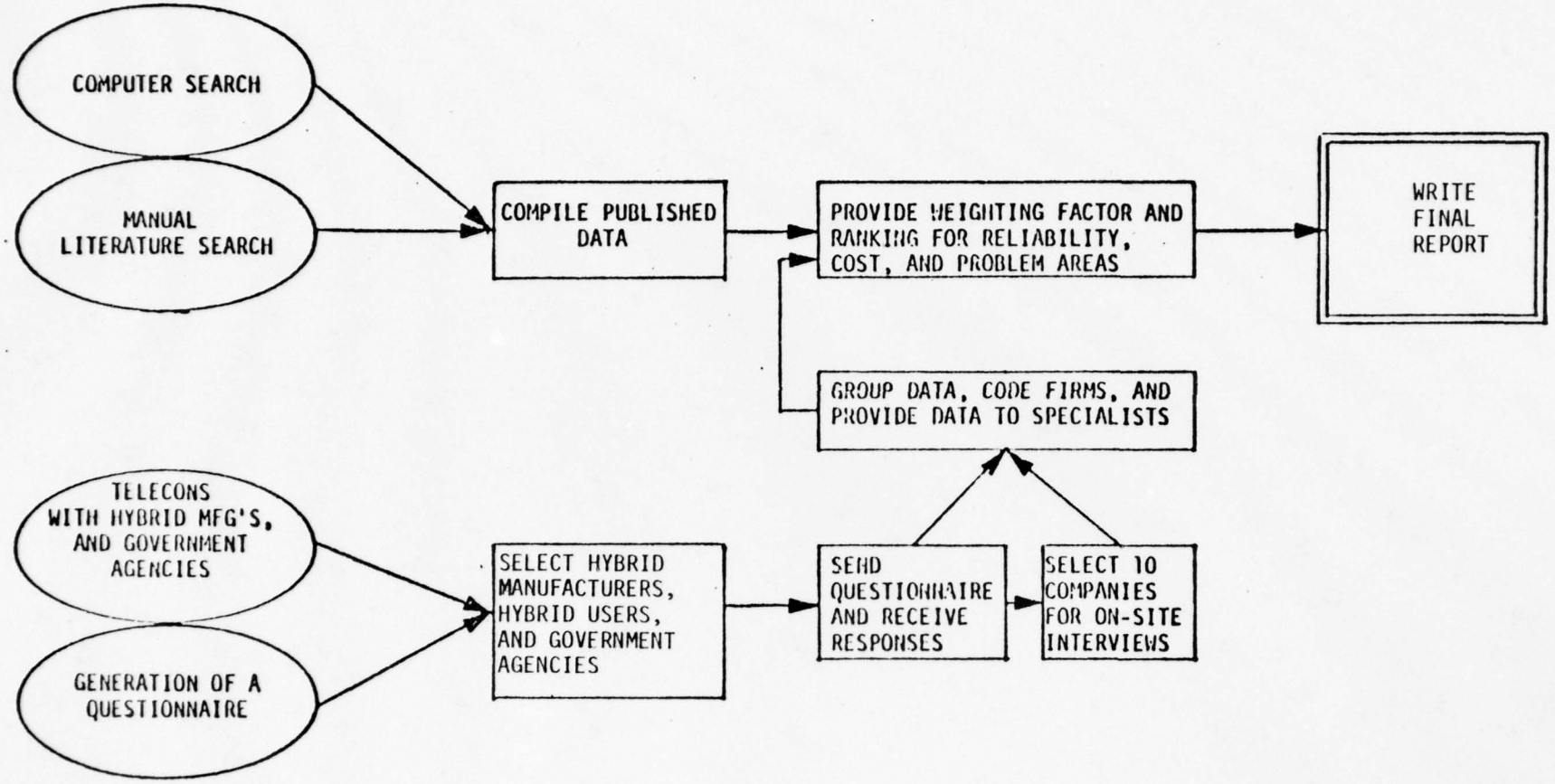

Figure 1. Hybrid Information Sources and Flow Diagram

4.0 LITERATURE SEARCH AND ANALYSIS

The objective of this portion of the study was to conduct both a computer-controlled and manual literature search of all publications and conference presentations on the subjects of hybrid microelectronics, hybrid microcircuits, thick film circuits, and thin film circuits for the past three years — 1975, 1976, 1977 — to collate the data in specific subtopics and to draw conclusions on trends in research and development of hybrid microcircuits, cost factors, and reliability problems.

4.1 Computer Search

The computer search was performed using the INSPEC, Science Abstract Index for the Electrical Category B. It should be noted that a computer search of other categories (e.g., Physics or Computer) or of other indices undoubtedly would have resulted in many more articles but the present search was considered representative. Of the 388 articles that resulted from the search, five were either strictly device oriented or were not applicable to hybrids and were excluded leaving a total of 383 abstracts. These were then collated into ten general subjects with the number of papers treating each subject recorded (see Table 1). If an article covered more than one subject, it was counted several times. Hence, the total number of subject articles expanded to 465. The ten general topics were then further subdivided into more specific topics. The number of articles for each subtopic is given in Tables 2 through 11. Abstracts of the references used from the computer search are provided separately in Volume II.

4.1.1 Results and Interpretation of Results from Computer Search

The conclusions drawn from an analysis of papers and publications may be biased by a few prolific writers on a particular subject which may or may not be critical to hybrid cost or reliability. Conversely, subjects of vital interest are not necessarily reported in the open literature. Therefore, a large number of articles in one subject matter does not necessarily indicate the need for funding by the government. In fact, it

may indicate considerable interest and activity on the part of industry and that industry will continue to sponsor those programs. It is therefore important that the results of the literature search be considered together with the questionnaire and survey results. However, assuming that the quantity of technical articles is related to activity and concern in the hybrid microcircuit industry, the following may be stated.

(1) The number of articles in thick film circuits (153) was about equal to the number in thin films (156) indicating about equal activity in both areas, and each constituting about 33% of the total articles.

(2) The number of foreign articles was 55% of the total. This probably does not indicate disproportionate off-shore activity in hybrid microcircuits because most of the articles were of a review, general, or tutorial nature.

(3) A preponderance of thin film articles was concerned with specific circuit applications rather than technology. This was less true of thick films and is not surprising considering the maturity of the thin film process relative to that of thick films.

(4) For thin films, besides circuit applications which comprised the largest number of papers, there was considerable emphasis on resistors, deposition methods, and production methods.

(5) The next biggest category after thick and thin films was that of interconnections (7%) followed by design, failure modes and mechanisms and testing, each of which was also about 7%.

(6) In the articles on testing, there were as many test methods as there were articles. There was no particular emphasis or extensive work on any one test method. This could be an indicator of confusion in testing and may suggest a need for guidelines or standardization.

(7) In thick films, besides articles on circuit applications and general review articles, the next two biggest categories dealt with resistors and conductors.

(8) The articles on interconnections were fairly evenly spread over a number of subtopics but the two areas receiving the most attention were Al wire bonding and solder attachment.

(9) Other categories containing six or more papers included computer-aided design, moisture and moisture effects, wire bonds, contamination, epoxy attachment, and alumina substrates.

TABLE 1. MAIN TOPICS AND NUMBERS OF ARTICLES FOR EACH TOPIC

Thick Films	153
Thin Films	156
Interconnections	33
Attachment	9
Design	28
Failure Modes/Mechanisms	24
Encapsulants/Coatings	10
Package Sealing	7
Substrates	22
Testing	24
Total	465

TABLE 2. *THICK FILM SUBTOPICS*

Conductors	24
Resistors	27
Capacitors	5
Multilayering	7
Equipment (10 articles are concerned with screens)	16
Circuit Applications	48
Review/General Articles	25
Microstructural Studies	1
Total	153

TABLE 3. THIN FILM SUBTOPICS

Conductors	9
Resistors	24
Capacitors	5
Deposition Methods	12
Circuit Applications	77
Review/General Articles	8
Production Experience	12
Photoetching	3
Analysis	4
Other (Structure and Properties)	2
Total	156

TABLE 4. INTERCONNECTIONS

Automated Bonding	2
Ribbon Wire	3
Al Wire Bonding	7
Au Wire Bonding	3
Beam Leads	4
Crossover Systems	4
Solder Attachment	7
Lead Frame Attachment	1
Berg Connectors	1
Wire Bond Strengths	1
Total	33

TABLE 5. ATTACHMENT (DEVICES/SUBSTRATES)

Epoxy Attachment	7
Alloy/Eutectic Attachment	2
Total	9

TABLE 6. DESIGN

Computer Aided Design	13
Standardization	3
High Density Circuits	5
Specifications and Guidelines	3
Thermal Dissipation	4
Total	28

TABLE 7. FAILURE MODES/MECHANISMS

Moisture and Moisture Effects	4
Electromigration	3
Adhesion	3
Contamination/Corrosion	6
Wire Bonds	7
Beam Leads	1
Total	24

TABLE 8. ENCAPSULANTS/COATINGS

Glassivation	4
Plastic Encapsulation	4
Organic Coatings	2
Total	10

TABLE 9. PACKAGE SEALING

Low Temperature Seam Sealing	1
Solder Sealing	1
Projection Resistance Welding	1
Epoxy Sealing	1
Packages for Thick Film Circuits	2
Encapsulation	1
Total	7

TABLE 10. SUBSTRATES

Printed Circuit Epoxy	1
Polyimide	3
Micaply	1
Large Area Substrates	2
Substrates With Vias	5
Fused Silica	1
Alumina	9
- Physical Defects in	
- Laser Cutting	
- Bowing After Multilayering	
- Surface Characteristics	
- With Cr_2O_3 and MgO Additives	
Total	22

TABLE 11. TESTING (ELECTRICAL AND SCREEN TESTS)

Hermeticity	1
Adhesion of Thin and Thick Films	3
Qualification (of Thick Film Pastes)	2
Wire Bond Tests	1
Photoresist	1
Accelerated Life Tests	1
PIND	1
Electrical	2
Solderability	1
Visual	1
IR Scanning Microscope	1
Halography	1
Fault Diagnosis (Computer Aided)	1
Backscatter Spectroscopy	1
Auger Spectroscopy	1
Thermal (by IR Radiation)	1
Temperature Distribution (Computer Aided)	1
X-ray Diffraction Stress Analysis	1
Ion Microprobe Analysis of Contaminants	1
Stress Wave Emission Analysis for Microcracks	1
Total	24

4.2 Manual Search

In addition to the computer search, a manual search and review was made of articles presented in 1977 at ISHM, Reliability Physics Symposium, COMPCON, IEEE Electrical Insulation Conference and American Vacuum Society/ISHM; and in 1976 at the Army Hybrid Microcircuit Symposium. In this search, 100 articles were assessed and classified into 11 general categories. Articles that covered more than one subject were included in several categories.

4.2.1 Results of Manual Search

Twenty-four percent (the largest %) of the articles was in the area of thick film circuits. Thin film articles, however, were sparse (only 7 out of 102). After thick films, the next largest category dealt with interconnections and bonding (20%), followed by failure analysis (12%), tests and quality control (9%), and design (9%). A list of the categories and number of papers per category is given in Table 12. It is interesting that, as with the computer search, the second biggest category was again interconnection/bonding and the third, fourth, and fifth categories were failure analysis tests, screen tests and design factors. A bibliography of references used in the manual search is given in Appendix A.

TABLE 12. TOPICS OF CONFERENCE PAPERS AS INDICATORS OF INDUSTRY EMPHASIS IN HYBRID MICROELECTRONICS

Thick Films (24)

Conductor Characterization (1)
Conductor Adhesion (2)
Qualification (2)
Resistor Trimming (3)
Resistor Characterization and Reliability (5)
Large Area Substrates (3)
Multilayer Thick Films (3)
Thick Films on BeO Substrates (2)
Polymer Thick Films (1)
Fine Line Printing (1)
Applications (1)

Thin Films (2)

Photoresist Testing (1)
Conductor Spray Coating (1)

Interconnections (20)

Tape Carriers (8)
Automated Wire Bonding (1)
Beam Lead Bonding (2)
Bump Bonding (3)
Chip Carriers (2)
Wire Bonds (3)
Spider Bonding (1)

Failure Analysis (12)

Moisture Problems (9)
Electrical Shorts (1)
Beam Lead Fatigue (1)
General Failure Modes (1)

TABLE 12 (cont)

Tests/Quality Control (9)

Hermeticity (1)
Qualification and Quality Control (3)
Wire Bonds (2)
Photoresist (1)
PIND (2)

Design (9)

Package Design (2)
High Density Packaging (1)
Large Scale Hybrids (1)
CAD (1)
Optical Coupling (1)
Power Hybrids (2)
High Temperature (300°C) (1)

Attachment Materials and Processes (5)

Epoxies (5)

Substrates (5)

Insulated Metal (1)
BeO (2)
Pyrolytic Boron Nitride (for MICs) (1)
Ceramic-Impregnated Teflon (for MICs) (1)

Coatings and Encapsulants (4)

General Encapsulants (3)
Particle Immobilizing Coatings (1)

Microwave Circuits (9)

Substrates for (3)
Design (4)
Processes (2)

Other Categories (9)

Cleaning (1)
Standard Electronic Modules (SEM) (2)
Packaging and Sealing (5)
Yield Improvements (1)

TABLE 12 (cont)

Design (10)

Package Design (1)
High Density Packaging (1)
Large Scale Hybrids (3)
CAD (1)
Optical Coupling (1)
Power Hybrids (2)
High Temperature (300°C) (1)

Attachment Materials and Processes (6)

Epoxies (4)
Solder (1)
Impurities in Au/Sn Preforms (1)

Substrates (5)

Alumina (2)
Insulated Metal (1)
BeO (2)

Coatings and Encapsulants (4)

General Encapsulants (3)
Particle Immobilizing Coatings (1)

Microwave Circuits (9)

Substrates for (3)
Design (5)
Filters (1)

Other Categories (7)

Cleaning (1)
Standardization (SEM) (1)
Packaging and Sealing (4)
Yield Improvements (1)

5.0 SURVEY

A survey of hybrid microcircuit cost and reliability factors and state-of-the-art technology was performed by both a questionnaire and selected on-site visits.

A "Hybrid Microcircuits Cost and Reliability Survey" questionnaire was prepared and sent to 38 firms. The firms represented a broad cross-section of those involved in hybrid microcircuits and included manufacturers, users, government agencies, and universities. A list of the firms and their addresses is given in Table 13. Completed questionnaires were received from 30 of the 38 firms. On-site visits were made to the 10 firms listed below:

Company	Address
McDonnell Douglas	St. Charles, MO
Electronic Communications, Inc.	St. Petersburg, FL
Honeywell	St. Petersburg, FL
Norden	Norwalk, CT
Micropac	Garland, TX
Sandia Laboratories	Albuquerque, NM
Hughes	Fullerton, CA
Hughes	Newport Beach, CA
General Dynamics	Pomona, CA
Beckman Instruments	Fullerton, CA

5.1 Questionnaire

The questionnaire was structured into eleven sections. The first three sections contained general questions directed primarily to the manager of the Hybrid Microelectronics Department or one of his staff engineers who has cognizance over all facets of the hybrid activity. The remaining sections dealt with specific technical areas and were directed to experts in these areas (a copy of the questionnaire is given in Appendix B).

For purposes of the questionnaire, a hybrid microcircuit was defined as a film circuit to which discrete active and/or passive components have been added. These discrete components can be single resistors, capacitors, transistors, diodes, inductors, and silicon or sapphire integrated circuits

TABLE 13. FIRMS THAT RECEIVED QUESTIONNAIRE

Firm	Address
Kaiser Electronics	1681 Page Mill Rd. Palo Alto, CA 94306
John Hopkins Univ. Applied Physics Lab.	8621 Georgia Ave. Silver Springs, MD 20910
Westinghouse System Development Div.	P.O. Box 746 Baltimore, MD 21203
Tektronix, Inc.	P.O. Box 500 Beaverton, OR 97077
Sperry Flight Systems	P.O. Box 21111 Phoenix, AZ 85036
Sandia Laboratories	P.O. Box 5800 Kirtland AFB, NM 87115
Rockwell Internat'l. Space Division	12214 Lakewood Blvd. Downey, CA 90241
Rockwell Internat'l. Electronic Devices Div.	P.O. Box 10462 Dallas, TX 75207
Rockwell Internat'l. Electronic Devices Div.	P.O. Box 4192 Anaheim, CA 92803
Raytheon Corporation Missile Systems Div.	Hartwell Rd. Bedford, MA 01780
McDonnell-Douglas Electronics Co.	P.O. Box 426 St. Charles, MO 63301
Hughes Aircraft Co. Ground Systems Div.	P.O. Box 3310 Fullerton, CA 92634
Hughes Aircraft Co. Microelectronics Div.	500 Superior Ave. Newport Beach, CA 92663
Honeywell Avionics Div.	13350 U.S. Highway 19 St. Petersburg, FL 33733
Bendix Corporation	P.O. Box 1159 Kansas City, MO 64141
United Technologies, Norden Division	Helen St. Norwalk, CT 06856

TABLE 13 (cont)

Firm	Address
*Beckman Instruments, Inc. Helipot Division	2500 Harbor Blvd. Fullerton, CA 92634
Hewlett Packard Co. Loveland Division	815 Fourteenth St. Loveland, CO 80537
*Litton Data Systems Div.	8000 Woodley Ave. Van Nuys, CA 91409
General Dynamics, Pomona Division	P.O. Box 2507 Pomona, CA 91766
Applied Technology, Division of ITEK	525 Almanor Ave. Sunnyvale, CA 94086
Army/MIRADCOM	Redstone Arsenal Huntsville, AL 35809
Magnavox	2329 Maricopa Torrance, CA 90503
GTE, Sylvania Electronic Systems Group	P.O. Box 188 Mountain View, CA 94042
Micropac	905 E. Walnut St. Garland, TX 75040
University of So. Florida	Tampa, FL 33620
Intermedics, Inc.	P.O. Box 617 Freeport, TX 77541
NASA, Johnson Space Flight Center	Houston, TX 77058
NASA, Marshall Space Flight Center Astrionics Division	Marshall Space Flight Center AL 35812
Army/ECOM Electronics Technology & Devices Lab.	Ft. Monmouth, NJ 07703
*RADC	Griffiss Air Force Base NY 13441

TABLE 13 (cont)

Firm	Address
*Aerospace Corporation	P.O. Box 92957 Los Angeles, CA 90009
TRW Systems Group	One Space Park Redondo Beach, CA 90278
*Texas Instruments	Dallas, TX
*Northrop Electronics	2301 West 120th St. Hawthorne, CA 90250
*Hewlett Packard Co.	1900 Garden of the Gods Road Colorado Springs, CO 80907
*Hewlett Packard Co.	1400 Fountain Grove Pky. Santa Rosa, CA 95401
ECI, Division of E-Systems	P.O. Box 12248 St. Petersburg, FL 33733

*Indicates questionnaires not returned.

or any combination of these devices. The circuits may be packaged or unpackaged but were assumed to be packaged unless otherwise indicated. The main interest was in circuits fabricated on ceramic substrates.

5.2 Results of Questionnaire

The responses to selected questions from the questionnaire that were considered most important were collated and are presented in Tables 14 through 36. Brief summaries are given for each table. These results provide insight into the major cost and reliability factors as identified by industrial firms and government agencies and should be useful in defining and planning future programs that will result in substantial cost reductions and reliability improvements of hybrid microcircuits. Since, in some cases, sensitive information is given, the various companies are not identified but are listed by a Code Number (1 through 30). These numbers do not correspond to the listing of the companies in Table 13.

5.2.1 High and Low Cost Contributors in the Manufacture of Hybrid Microcircuits

Questionnaire recipients were asked to rank cost contributors and indicate the approximate percentage contribution of each to total hybrid cost. Eight categories (Questionnaire, Section II, Question 1) were recommended for ranking. Further, the recipients were also asked to identify and rank the major cost elements for each of the three categories they had ranked as the top cost contributors. The collated answers for these questions are given in Tables 14 through 18. In summary, the three highest cost contributors (Table 14) were reported to be Assembly and Packaging Processes (70% of firms reported), Fabrication Materials and Devices (67%), and Electrical Testing (40%). The categories ranked as lowest cost contributors were Screen Testing, Substrate Fabrication Processes, Documentation and Customer Interface, and Rework (Table 15).

Key cost factors for the Fabrication Materials and Devices category were Active Devices (including ICs, MOS/LSI, and transistors) and Packages (Table 16). Other high cost elements for this category were custom capacitors and resistors, noble metals, and substrates. In the Assembly and Packaging Processes category, the key cost factors reported were Wire Bonding, Device and Substrate Attachment, and Sealing (Table 17). Other high cost

TABLE 14. HIGH COST CONTRIBUTORS AND APPROXIMATE PERCENTAGE CONTRIBUTION TO TOTAL HYBRID COST

Company Code No.	Quality Control/ Quality Assur.	Fabrication Matls./Devices	Electrical Test	Assembly & Packaging Processes	Rework	Substrate Fabrication Processes	Documentation & Customer Interface	Screen Testing
1		1 (30%)	2 (20%)	3 (10%)				
2		1 (28%)	2 (20%)	3 (19%)				
3		1 (30%)	2 (25%)	3 (10%)				
4	2 (15%)	1 (30%)			3 (12%)			
5		1 (25%)		2 (23%)		3 (20%)		
6		1 (35%)		2 (25%)	3 (15%)			
7	1 (20%)	2 (18%)		3 (15%)				
8		2 (15%)	3 (15%)	1 (20%)				
9	2	3		1				
10	2		3				1	
11	3 (20%)	2 (20%)		1 (40%)				
12		3 (20%)		1 (30%)			2 (20%)	
13			3	1	2			
14	1 (55%)		2 (20%)	3 (7%)				
15			1 (15%)					2 (10%)
16			1 (25%)				3 (15%)	2 (15%)
17		2 (20%)			1 (30%)			
18		2 (16%)		1 (20%)			3 (15%)	
19	3 (18%)		1 (25%)	2 (20%)				
20	3	1						2
21 (NR)								
22		1 (40%)	2 (20%)	3 (15%)				
23		1 (50%)		2 (15%)		3 (10%)		
24	3 (20%)						1 (20%)	3 (20%)
25 (NR)								
26		1 (45%)		2 (20%)	3 (16%)			
27			3 (15%)	2 (18%)			1 (20%)	
28		2		1		3		
29		1 (25%)		3 (18%)			2 (23%)	
30		2 (25%)		1 (25%)				3 (15%)

NR = no response; NA = not applicable

TABLE 15. LOWER COST CONTRIBUTORS (<5% CONTRIBUTION TO TOTAL HYBRID COST)

Company Code No.	Documentation & Customer Interface	Substrate Fabrication Processes	Screen Testing	Quality Control/ Assurance	Rework	Design	Electrical Test	Fabrication Materials
1		X	X					
2			X	X				
3	X	X	X					
4	X	X	X					
5	X			X	X			
6			X			X	X	
7	X		X		X			
8	X		X		X			
9	X	X					X	
10		X			X			X
11	X	X					X	
12			X	X	X			
13	X	X	X					
14	X		X					X
15 (NR)								
16		X		X	X			
17	X	X						
18		X		X			X	
19		X	X		X			
20	X	X			X			
21 (NR)								
22	X		X	X				
23	X		X	X	X			
24		X			X			X
25 (NR)								
26			X				X	X
27			X					
28 (NR)								
29			X		X			
30				X	X		X	

TABLE 16. MATERIALS/DEVICES THAT ARE KEY COST CONTRIBUTORS AND PERCENTAGE CONTRIBUTION

Company Code No.	Beam Lead Devices	RF Transistors	Integrated Circuits	Custom Resistors	Active Devices*	Packages	Capacitors	Substrates	Noble Metals
1		1 (50-80%)	2 (50-70%)		3 (30-50%)				
2			1 (70%)	2 (30%)					
3					1 (65%)	2 (20%)			
4					1	2	3		
5					1 (6-20%)	2 (6-15%)			
6					2 (10%)	1 (15%)			3 (5%)
7			1 (30-50%)		2 (20-30%)	3(10-15%)			
8					2 (30%)	1 (50%)	3 (20%)		
9					1				
10 (NA)									
11			1 (60%)			2 (25%)			3 (15%)
12					2 (30%)	1 (50%)			3 (20%)
13 (NA)									
14 (NA)									
15 (NA)									
16			1 (50%)			2 (25%)		3 (25%)	
17	1 (70%)							2 (30%)	
18			1 (75%)			2 (15%)		3 (10%)	
19 (NA)									
20			1			2	3		
21 (NR)									
22			2 (30%)			1 (50%)			
23					2 (30%)		1 (30%)		3 (20%)
24 (NA)									
25 (NR)									
26					2 (30%)	1 (35%)			
27 (NA)									
28			2	3	1				
29					1 (50%)	3 (15%)	2 (15%)		
30				3 (15%)		2 (25%)		1 (50%)	

*Active devices other than integrated circuits such as transistors, diodes, MOS/LSI, etc.

TABLE 17. ASSEMBLY PROCESSES THAT ARE KEY COST CONTRIBUTORS AND PERCENTAGE CONTRIBUTION

Company Code No.	Soldering	Substrate & Device Attachment	Wire Bonding	Sealing	Wire Bond Pull Test	In-Line Inspection	Cleaning/ Handling
1	1 (50%)	2 (25%)	3 (10%)				
2 (NR)							
3		2 (35%)	1 (45%)	3 (10%)			
4 (NA)							
5			1 (30-50%)			3 (20%)	2 (30%)
6		2 (6%)	1 (10%)	3 (4%)			
7		2 (15-25%)	1 (30-70%)	3 (10-15%)			
8		2 (30%)	1 (50%)				
9		2 (30%)	1 (40%)				3 (20%)
10 (NA)							
11			1 (70%)	3 (10%)		2 (20%)	
12		2 (20%)	1 (50%)				
13	2		1	3			
14		2 (20%)	1 (25%)	3 (20%)			
15 (NA)							
16 (NA)							
17 (NA)							
18		2 (30%)	1 (50%)				3 (20%)
19		2 (30%)	1 (60%)	3 (10%)			
20 (NA)							
21 (NR)							
22		1 (30%)	2 (20%)	3 (15%)			
23		1 (80%)					
24 (NA)							
25 (NR)							
26			1 (20%)				
27		3 (20%)	2 (30%)		1 (50%)		
28		3	1	2			
29		3 (10%)	2 (15%)			1 (20%)	
30		2 (25%)	1 (50%)	3 (15%)			

elements included In-Line Inspection and Cleaning and Handling. For the third high cost category (Electrical Testing) the two main cost factors were reported to be high-low temperature testing and high-low-nominal voltage testing (Table 18). A summary of all key cost factors is given in Figure 2.

5.2.2 Cost of Military Hybrids Compared to Commercial Hybrids

The responses to the question of what factors make hybrids of comparable complexity more expensive when they are produced for military applications than for commercial applications are summarized in Table 19. The majority of the firms reported that Screen Tests and Test Requirements, and Documentation and Record Keeping were the key cost factors. Other major reasons identified for the higher cost of military hybrids as compared to commercial hybrids included inspection, material limitations, and requirements for specification grade components. Among the material limitations mentioned were the requirements for the use of hermetic packages (gold-plated metal packages) and for the use of eutectic alloy in attaching die and substrates.

It is interesting to note that screen testing was ranked by a majority of firms as among the lower cost contributors to the total cost of hybrids (Table 15), but ranked as one of the top two factors that contributed most to the additional cost of military hybrids. The interpretation of this apparent inconsistency may be that when answering the general question concerning major cost contributors, both military and commercial hybrids were considered and the performance of screen tests was not generally considered to be a costly item. However, when comparing the cost of military to commercial hybrids, the additional screen testing and resultant yield loss becomes a major cost element.

5.2.3 Reliability of Hybrid Microcircuits

Several questions concerning the reliability of hybrid microcircuits were asked. These included the following:

(a) What do you consider to be the key factors affecting the reliability of hybrid microcircuits?

(b) What do you consider to be the top persistent failure modes in hybrid microcircuits?

TABLE 18. SPECIFIC ELECTRICAL TESTS OR TEST FACTORS THAT ARE KEY COST CONTRIBUTORS

Company Code No.	Temperature Tests	Preseal 1st Functional	Final Test	Environmental Tests	Hi-Lo-Nominal Voltage Testing	Tight/ Difficult Specification	Poor Design for Testing	Fault Isolation	Data Read/ Record	Dynamic Tests
1	1 (66%)			2 (20%)	3 (14%)					
2						1 (50%)	2 (50%)			
3								1 (85%)		
4 (NA)										
5 (NA)										
6 (NA)										
7 (NA)										
8					1 (40%)					
9 (NA)										
10	1 (10%)									2 (10%)
11 (NA)										
12 (NA)										
13 (NR)										
14						1 (70%)				
15	1 (15%)									
16	1 (75%)									
17 (NA)										
18 (NA)										
19	1 (60%)				2 (30%)					
20 (NA)										
21 (NR)										
22		2 (20%)	1 (80%)							
23 (NA)										
24 (NA)										
25 (NR)										
26 (NA)										
27					1 (75%)					
28 (NA)										
29 (NA)										
30 (NA)										

Fabrication Materials & Devices	- Active Devices, ICs, MOS/LSI, transistors. - Packages - Custom Resistors, Capacitors, Noble Metals, Substrates
Assembly & Packaging Processes	- Wire Bonding - Device and Substrate Attachment - Sealing - In-line Inspection - Cleaning/Handling
Electrical Testing	- Hi-Low Temperature Testing - Hi-Low-Nominal Voltage Testing - Fault Isolation

Figure 2. Summary of Cost Drivers for Hybrid Microcircuits

TABLE 19. FACTORS THAT MAKE HYBRIDS OF COMPARABLE COMPLEXITY MORE EXPENSIVE WHEN THEY ARE PRODUCED FOR MILITARY USE THAN FOR COMMERCIAL USE

	Company Code No.																													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21 NR	22	23	24	25	26	27	28	29	30
Documentation/ Keeping Records	X	X		X		X	X		X	X			X	X				X	X				X	X		X		X	X	X
Qualification												X												X	X					X
Process Limits & Test Requirements	X																												X	
Low Volume	X												X												X					
Operating Limits (Temp./Shock/ Vibration)	X																											X		
Screen Tests & Test Requirements*		X	X	X	X	X	X	X	X	X	X				X	X	X	X	X			X		X	X	X	X			X
Inspection		X	X	X							X			X	X			X	X	X		X	X	X						
Limitation on Rework			X		X			X						X																
Requirement for Spec. Components			X				X							X		X		X		X		X					X			X
Material Limitations**					X	X		X			X				X		X	X	X	X		X								

*Yield losses due to screens; too many screen tests and other tests; temperature testing of electricals.

**Hermetic package, gold-plated packages, eutectic attach instead of epoxy.

(c) Should the government sponsor more basic failure mechanism studies; and if so, in what specific areas?

The responses to these questions are given in Tables 20, 21 and 22, respectively.

The major factors affecting hybrid reliability (Table 20) were identified as active device chips (15 of 30 companies); wire bonds (11 companies); control of materials, components and processes (10 companies); poor design practices (9 companies); moisture and other contaminants (8 companies; and seal integrity (6 companies).

Two predominant categories were identified as top persistent failure modes. Twenty-five of the 30 companies (83%) reported wire bonds, and 24 of the 30 companies (80%) reported defective semiconductor devices. Other major categories were contamination (13 of the 30 companies), and moisture related (7 of the 30 companies). If contamination is grouped together with moisture, because most contamination-related failures require the presence of moisture, then this category becomes the third most important (20 out of 30 companies). Other significant failure modes reported included leaky packages, defective capacitors, and film metallization problems. (Table 21.)

As shown in Table 22, 25 of the 30 companies (83%) felt that the government should sponsor more basic failure mechanism studies and recommended 23 study areas. Areas recommended most frequently were Sources of Moisture/Moisture Effects/Moisture Control (8 companies), Particle Contaminant Effects and Contamination Sources (7 companies), Wire Bond Failure Studies (7 companies), and Materials Compatibility Study (7 companies).

5.2.4 Tape Automated Bonding

When queried as to whether or not they felt that the tape carrier approach to automated bonding will substantially benefit the assembly of military hybrids, the majority of the companies answered that they did (17 yes, 10 no, see Table 23). However, those that answered yes generally qualified their answer that tape carrier is best suited to high volume and to less complex circuits. The main advantages cited were pretesting and burn-in capabilities with resulting higher reliability. Several of the respondees expressed serious concern about the availability of a wide range of devices in tape carrier form and believe that the military hybrid industry will have the same problems as they had with beam-leaded devices.

TABLE 20. KEY FACTORS AFFECTING THE RELIABILITY OF HYBRID MICROCIRCUITS

	Company																													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Complexity	X		X													X														X
Technology Used	X									X															X					
Control of Materials, Components & Processes Used	X	X	X			X							X	X				X					X	X						X
Nonstandardization of Requirements/Poorly Defined Specs.		X									X																			
Operating Environment			X												X															
Seal Integrity			X						X						X	X											X	X		
Wire Bonds				X				X	X			X				X	X				X	X					X	X	X	
Moisture/Contaminants				X		X						X					X		X	X								X	X	
Capacitor Delamination				X																										
Active Device Chips					X		X	X	X			X					X	X	X	X	X			X		X	X	X	X	
Screening and Test Practices						X																			X					X
Poor Design Practices (Electrical Margins, Physical Tolerances)						X	X			X			X									X		X	X	X			X	
Workmanship							X				X		X																	X
Rework								X																						
Interconnect Techniques										X						X														
Materials Incompatibility										X				X																
Process Sequence																					X									
Thick Film Resistor Instability																							X							
Device Attachment																				X										

TABLE 21. TOP PERSISTENT FAILURE MODES IN HYBRID MICROCITCUITS

	Company Code No.																												
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Resistor Drift																							X			X				
Ceramic Cracking																							X							
Wire Bonds	X	X	X	X		X	X	X	X	X	X	X	X	X		X	X	X	X		X	X		X	X	X	X	X	X	
Defective (Active) Semiconductor Devices	X		X	X	X	X	X		X		X	X		X			X	X	X	X	X	X	X	X	X	X	X	X	X	X
Defective Capacitors	X												X							X										
Leaky Packages		X						X								X				X		X		X						
Contamination			X			X	X	X	X			X	X				X	X	X	X							X		X	
Moisture Related				X		X	X			X					X			X		X										
Film Metallization Failures							X			X						X														
Solder Reflow														X																
Chip Attach														X																
Failures Temp. Extremes															X															
Centrifuge & Temp Cycle Failures																						X								
Static Zap																												X		

TABLE 22. SHOULD THE GOVERNMENT SPONSOR MORE BASIC FAILURE MECHANISM STUDIES; AND IF SO, IN WHAT SPECIFIC AREAS?

	Company Code No.																												
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Yes	X	X	X	X	X	X	X	X		X	X		X	X	NR	X		X	X	X	X	X	X		X	X	X	X	X	X
No									X			X					X							X						
Proposed Programs																														
Study Failures as Function of Technology Used or Controls Exercised	X																												X	
Wire Bond Failure Studies		X		X																	X	X			X	X	X			
Particle Contaminant Effects & Contamination Sources			X								X			X				X	X						X		X			
Reliability of Non-hermetic Hybrids (Passivated)			X																											X
Reliability of Tape Carried Devices			X																											
Source of Moisture/Moisture Effects/Moisture Control				X		X	X				X							X	X						X			X		
CMOS Failure Modes				X																						X				
Correlate Power Limits for Specific Devices & Attachment Methods					X																									
Materials Compatibility						X				X						X		X	X		X									X
Thermal Characterization						X																								
Thick Film Resistor Stability							X									X														
Effect of Screen Tests on Ultimate Reliability							X																							
Packaging, Sealing, Failures								X										X				X				X				
Chip Testing/Screening								X												X										
Stability of Metallization on Substrates										X	X																			
Effect of Binder & Additives to Thick Film Pastes											X															X				
Surface Preparation														X																
Basic Metallurgical Studies														X																
Cleaning																			X			X								
Capacitor Failure Mechanism																				X										
Leakage & Migration Causes																				X										
Temperature Runaway																						X								
Ceramic Failure vs Physical Properties																							X							

TABLE 23. WILL THE TAPE CARRIER APPROACH TO AUTOMATED BONDING SUBSTANTIALLY BENEFIT THE ASSEMBLY OF MILITARY HYBRIDS?

Company Code No.	Yes	No	Comments
1		X	Not for low volume and multiple part number per hybrid and special design die.
2	X	X	Yes: High reliability; No: High non-recurring costs.
3	X		Eliminates in-process rework for complex hybrids; reduces cost for high volume.
4	X		Pretest capability, eliminates wire bonding, face up gives inspectability, available in unlimited number of device types.
5		X	Except for high volume, most military systems require less than 5000 circuits.
6	X		Permits testing and burn-in of devices prior to assembly; volume must be high.
7		X	Complex patterns; loss of real estate; problem obtaining custom MOS in tape carrier.
8 (NR)			
9		X	Requires high volume.
10	X		Higher bond strengths, testable chips, less operator dependency.
11	X		Especially for high volume - Reliability should improve.
12 (NR)			
13	X		Depends on circuit. Uniform hybrids such as digital memories would benefit.
14	X		Testability and Temperature screen prior to assembly; eliminates chip and wire.
15 (NR)			
16		X	Military hybrids are generally low volume; tape carrier best suited for very high volume and few circuit types.
17	X		Only if semiconductor manufacturers will sell devices in tape carrier form.
18	X		No comments.
19	X		Only if carriers are available and as low cost as chips are now - only if bonding machines can be developed to use individual devices rather than reels.
20	X		Only if volume can justify set-up charges; will require convincing.
21	X	X	Ease in handling, burn-in, testing; but expensive and problems of inner-lead bond reliability and inspectability.
22		X	Designers do not leave enough range of selection.
23		X	Because of small quantities.
24		X	Availability will be same as for beam-leaded devices. Military devices represent only small portion of semiconductor business.
25 (NR)			
26	X		No Comments
27	X		Only for high volume requirements.
28 (NR)			
29	X		Will require large investment by hybrid facilities, or a good support industry to provide chips on tape.
30	X		Provides higher yields, reliability, and reproducibility in large quantity hybrid applications.

5.2.5 Studies To Which Companies Are Committing Discretionary Funds

The hybrid technology areas to which the various companies are presently committing or are planning to commit their discretionary funds (burden, IR&D, etc.) are listed in Table 24. As shown in this Table, 21 companies are conducting or are planning to conduct studies in 32 different areas. Five companies are conducting studies of Tape Carrier Assembly while three each are conducting studies related to Large Area Multilayer Hybrids, Low Cost Hybrid Designs and CAD, Base Metal Thick Film Conductors, Bonding and Attachment, Automatic Wire Bonding, and High Density Multilayer Thick Films. Undoubtedly, there is considerable overlap in the studies being conducted by the various companies but this cannot be determined from the information reported. However, as indicated, there is considerable activity in the hybrid area and companies are committing their discretionary funds to the solution of the related problems.

5.2.6 Hybrid Microcircuit Studies Recommended by the Various Companies

The companies were solicited to recommend studies ranging from basic research to manufacturing technology that should be performed to reduce the cost or improve the reliability of hybrids. Requests for study recommendations were made both in the general section of the questionnaire that was directed to management, and in the sections of the questionnaire dealing with specific technology areas that were directed to the experts in these areas. The responses were separately collated and are presented in Table 25 and Tables 27 through 36. The programs recommended in response to the request in the general section of the questionnaire are listed in Table 25. Studies recommended in each of the specific areas (Computer Aided Design, Hybrid Design, Materials/Devices, Thin Films, Thick Films, Component/Substrate Attachment and Interconnect Bonding, Package Sealing, Electrical Testing, Quality Control/Quality Assurance, and Rework) are listed in Tables 27 through 36. As would be expected there is an overlap between the programs or studies recommended in Table 25 and those recommended in Tables 27 through 36.

As seen in Table 25, the thirty companies recommended 36 separate items that they feel require government funding for continued advancement in the

hybrid microcircuit state-of-the-art. Leading the list, with 16 firms making the same recommendation, was a study to Develop Low Cost, High Reliability Hybrid Packaging and Sealing Methods. The second major recommendation (10 firms) was to Develop Low Cost Automated Assembly Processes for Both Device Attachment and Wire Bonding. When the projects were grouped in general categories (Table 26), the top three subject areas were Interconnections, Testing, and Packaging/Sealing. A brief summary of the studies recommended in each of the specific areas (Tables 27 through 36) follows:

(a) Computer Aided Design (Table 27) - When asked if further advances in computer-aided design were necessary to reduce hybrid costs, 15 companies answered yes, five answered no, and 10 did not give an opinion. The two primary areas in which further effort was recommended were Automatic Placement/Layout (Artwork Generation) (11 firms) and Automated Documentation (5 firms).

(b) Hybrid Design (Table 28) - Sixteen of the 30 companies felt that the government should sponsor programs to standardize on design guidelines for industry while 13 felt it should not. Thermal Design and Layout Practices (Design Aids) received the most mention followed by Package Standardization, Size Standardization, and Large Area Hybrid Design. Other recommended studies included Reliability/Cost Versus Technology/Applications Tradeoffs, Cost Versus Density/Size Tradeoffs and Next Level Packaging. The latter study would be a necessary requisite for the Package Standardization study.

(c) Materials/Devices (Table 29) - The responses to the question on recommended programs for hybrid materials and devices was quite varied. Many companies erroneously recommended programs in device testing, assembly, and processes under this category. Twenty-four companies recommended 24 study programs. Nine of the studies dealt with substrate materials, seven were device related, three package related, and five were in miscellaneous categories. The studies most frequently recommended were Development of Low Cost Thick Film Metallization With Improved Bond Reliability (6 companies); Development of Finer Grained, Smoother, Alumina Substrates (4 companies); and Development of Improved Adhesives (3 companies). Interest was

also shown in the development of multilayer substrate materials (polyimide, cofired, thin film). In the device area, the primary emphasis was placed on developing the capability for testing and burn-in of devices at the chip level. In the packaging area, improved design and producibility, plating improvements and non-hermetic packaging were recommended for study. Moisture monitoring devices and contaminant protection coatings also were recommended for study by two firms each.

(d) Thin Films (Table 30) - A wide variety of studies were recommended (17 companies recommended 20 different studies) with generally no more than one company recommending a particular program. Most of the studies proposed were vague and appeared to be specific problems that a particular company was having rather than one that most companies were encountering. As examples, Automated Dynamic Resistor Trimming (a study recommended by 2 companies) is already being done by many firms and Improved Fixturing and Handling (recommended by one company) is generally not a problem. Three programs were exceptions, these were Development of a High Density Thin Film Multilayer Process (7 companies), Development of Processes to Batch Fabricate Wide Range Sheet Resistivity Materials on the Same Substrate (4 companies), and Development of High Stability Resistors and Resistor Passivation Coatings (4 companies). Other programs each recommended by at least two firms included evaluation of dry processing methods to replace wet chemical methods presently used, development of processes for conductors and resistors with finer lines and spacings (0.5 to 1.5 mils) in high yield, investigation of non-precious metal sputtered films as alternates to gold, and development of methods for sawing, separating, and inspecting ceramic substrates.

(e) Thick Films (Table 31) - A total of 24 studies were recommended by 17 companies. The following three studies were recommended most often (by 5 different companies): Evaluation of Non-Noble Metal Conductors, Development of Improved Resistor Inks, and Improvement of Conductor Adhesion and Wire Bondability.

(f) Component/Substrate Attachment and Interconnect Bonding (Table 32) - Chip and substrate attachment and device interconnections were reported among the top major contributors to high cost and poor reliability. In response to the question "What programs or studies in the areas of component attachment, substrate attachment, or interconnect bonding would you recommend?", 21 companies suggested 26 different studies. The study recommended most often (7 out of 21 companies) was Development of Tape Carriers With Alternate Device/Tape Bumping Methods. Other studies most frequently recommended were Development and Evaluation of Improved Adhesives, Development of Automated Wire Bonding, and Development of Improved Bond Characterization Techniques.

(g) Package Sealing (Table 33) - Seventeen of the 30 companies indicated that they do not have package sealing problems. The remaining 13 companies suggested 16 different studies. Five of the studies dealt with sealing methods and equipment, four each were concerned with sealing materials and analytical methods, two were concerned with package materials, and one with specifications and controls.

(h) Electrical Testing (Table 34) - The majority of the companies (20 out of 30) had no recommendations in this area. However, the 10 responding companies recommended seven programs, and five of the 10 companies recommended that work should be performed to Develop Automatic Fault Isolation Procedures.

(i) Quality Control/Quality Assurance (Table 35) - According to the responses of 24 firms, quality control/quality assurance activities account for an average of 20 percent of the total cost of a hybrid with a range of from 5 to 40 percent. Of the 30 firms queried, 18 responded that no study programs should be performed in the area of quality control/quality assurance while 11 firms suggested 12 programs. Development of Automatic Visual Inspection Techniques was the program most frequently recommended, followed by Development of In-Process Cleanliness and Moisture Monitors and 100% Pull Testing for Wire Bonds.

(j) Rework (Table 36) - In response to the questions as to whether they felt rework is essential in meeting cost and schedule requirements and whether they felt there is a need for standard rework procedures or guidelines, 27 of the 30 companies felt rework was essential and 19 felt that there is a need for rework procedures or guidelines. However, in spite of the fact that 90% of the companies felt that rework was essential, 50% (15 companies) felt that no additional studies were required in the area of rework. However, the other 15 companies recommended eight study areas. Of these, seven recommended a study to Establish Methods of Lid Removal/ Replacement, five recommended studies to Evaluate the Effect of Rework on Long Term Reliability and to Determine Rework Limitations and Establish Rationale, and four recommended a study to Establish Methods of Component and Removal and Replacement.

TABLE 24. HYBRID TECHNOLOGY AREAS TO WHICH DISCRETIONARY FUNDS ARE BEING COMMITTED

	Company																													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
									*				NR		*		NA	NA	NA	*	NA				NA					NR
Tape Carrier Assembly		X	X	X								X															X			
Thick Film Microstrip Circuits			X																											
Automatic Assembly			X																											
Large Area Multilayer Hybrids			X	X																			X							
Large Area Hybrid Packaging																							X							
Hermetic Chip Carriers and Leadless Carriers			X	X																										
Low Cost Hybrid Designs & CAD			X									X												X					
Moisture Effects				X																										
Ultrasonic Al Ball Bonding						X																								
Cluster Sealing						X																								
Base Metal Thick Film Conductors						X	X	X																						
Nitrogen Fired Resistors & Dielectrics							X																							
Stable Sputtered Resistor Systems							X																							
Package Sealing							X															X								
Bonding & Attachment							X			X													X							
Automatic Wire Bonding								X																			X	X		
Substrate Evaluation and Low Cost Substrates								X				X																		
Automatic Active Resistor Trimming								X				X																		
Assembly Mechanization (Chip Placement, Reflow Solder)								X																						
In Situ Thick Film Capacitors								X																						
Alternate Metallization Systems (Substrates)										X																				
New Interconnect Techniques										X																				
Thin Film Hybrids											X																			


Thick Film Microstrip Circuits
Automatic Assembly
Large Area Multilayer Hybrids
Large Area Hybrid Packaging
Hermetic Chip Carriers and Leadless Carriers
Low Cost Hybrid Designs & CAD
Moisture Effects
Ultrasonic Al Ball Bonding
Cluster Sealing
Base Metal Thick Film Conductors
Nitrogen Fired Resistors & Dielectrics
Stable Sputtered Resistor Systems
Package Sealing
Bonding & Attachment
Automatic Wire Bonding
Substrate Evaluation and Low Cost Substrates
Automatic Active Resistor Trimming
Assembly Mechanization (Chip Placement, Reflow Solder)
In Situ Thick Film Capacitors
Alternate Metallization Systems (Substrates)
New Interconnect Techniques
Thin Film Hybrids
Thin Film Resistors
Fine-Line Thick Films
Failure Analysis
Elimination of Packages
Elimination of Exposed Wire Bond Interconnections
Thin Film MICs
Thin Film Al Conductors
Epoxy Bonding
High Density Thick Film Multilayer

*None

TABLE 25. GENERAL RECOMMENDED HYBRID MICROCIRCUIT PROGRAMS

Recommended Program	No. of Firms Making The Recommendations	Suggested Category
Prepare military specifications strictly applicable to thick and thin film hybrid materials, processes and technology	2	Standardization
Standardize Semiconductor and Device Interconnection Methods	1	"
Generate MIL-Spec for Precious Metal Thick Film Pastes	1	"
Standardize Epoxies and Pastes. Verify the reliability and acceptability of polymeric materials in packages	4	"
Standardize Substrates and Packages, Sizes, and Configurations	5	"
Standardize Handling Techniques - to minimize electrostatic discharge, for fabrication	2	"
Standardize on Leak Testing Methods	1	"
Develop Low Cost Hybrid Packaging and Sealing Methods Including Polymer Seals, Molded Packages, Improved Coatings for Moisture Protection, and Plastic Encapsulation	16	R&D/Mantech
Correlate Sealing Techniques to Reliability and Provide Basis for Leak Rate Requirements. Elaborate on and simplify the calculation of hermeticity from the MIL-STD-883 equation.	5	R&D
Develop Hybridized SEM (Standard Electronic Module)	1	Development
Evaluate and Implement Non-noble Metal Conductors	5	R&D/Mantech

TABLE 25. (cont)

Recommended Program	No. of Firms Making Recommendation	Suggested Category
Evaluate and Establish Low Cost Improved Moisture Analysis Methods and Determine Moisture Threshold Levels for Hybrid Circuits	4	R&D/Mantech
Develop Better, Low Cost Die Evaluation/Testing Methods Prior to Assembly	5	Mantech
Correlate Field Reliability With Screen Tests, Determine Level of Screen Testing Requirement	4	R&D
Develop Better Nondestructive Tests	1	R&D
Evaluate Alternates or Improvement to PIND Test Including Particle Immobilizing Coatings	3	R&D/Mantech
Determine Effectiveness of Screen Tests: Centrifuge, Stress Testing	4	R&D
Develop Repair Processes for Circuits Failing PIND Test	1	Mantech
Establish Metal Migration Conditions and Limits	1	R&D
Develop Automated Precap Inspection Methods	1	R&D
Evaluate Low Cost Substrates, Enamelized Metal and Plastic Laminates	2	R&D/Mantech
Publish a Reliability Engineers' Handbook for Design and Reliability Prediction of Hybrid Devices	1	Development
Provide Ground Rules and Guidelines for Automated Layout Design	1	Development
Qualify Materials	1	Development
Evaluate and Select Optimum Cleaning Solvents, Processes, and Equipment for Contamination Control	4	Mantech

TABLE 25. (cont)

Recommended Program	No. of Firms Making The Recommendation	Suggested Category
Study and Characterize Thick Film Conductors, Resistors, and Dielectrics; Study Physics of Noise and Conduction Mechanisms	2	R&D
Develop High Density Thick Film Multilayer Process	1	R&D/Mantech
Develop Process and Materials for Multilayer Thin Film Circuits	1	R&D
Develop Batch Fabrication Process for High Sheet Resistivity Thin Films	2	Mantech
Define Processes and Equipment for Low Cost Automated Assembly Including Wire Bonding and Attachment	10	Mantech
Wire Bonding Studies: Obtain comparative data for thermosonic, ultrasonic, and thermocompression bonds; study ultrasonic aluminum ball bonding and effect of thick film conductors on wire bond reliability. Conduct wire bond failure mechanism studies.	7	R&D
Continue Work on Tape-Carried Devices for Hybrid Applications	2	R&D
Assess/Develop Methods to Eliminate Flying Wire and Wire Bonds	3	R&D
Evaluate Improved Aluminum Wire Alloys	1	R&D
Establish Reliability of Leadless Package Socket Interconnections	1	R&D
Develop Low Cost Process Monitoring Equipment (wire pull tester, etc.)	2	Mantech

TABLE 26. HYBRID MICROCIRCUIT PROGRAM SUBJECTS RECOMMENDED FOR GOVERNMENT SUPPORT, BY MAJOR CATEGORIES

General Category	No. of Firms Making Recommendations
Interconnections	24
Testing	22
Packaging/Sealing	22
Standardization	16
Thick Films	8
Thin Films	3
Other	13

TABLE 27. STUDIES RECOMMENDED IN COMPUTER-AIDED DESIGN

Company	Further Advances Required? Yes	No	Automatic Placement/Layout (Artwork Generation)	Automatic Resistor Pattern Generation	Automated Documentation	Microwave Circuit Analysis	Multilayer Short & Continuity Listings (Test Patterns)	Nodal Analysis of Geometric Layout	Thermal Models
1		X							
2		X							
3	X		X						
4		X							
5		X							
6 (NR)									
7	X			X					
8 (NR)									
9 (NR)									
10		X							
11 (NR)									
12	X		X		X				
13	X					X			
14	X		X		X				
15 (NR)									
16	X		X				X		
17	X		X						
18	X		X		X				
19	X		X		X				
20	X		X						
21 (NR)									
22 (NR)									
23	X			X					
24	X		X					X	
25 (NR)									
26	X		X						X
27 (NR)									
28 (NR)									
29	X				X				
30	X		X						

TABLE 28. STUDIES RECOMMENDED IN HYBRID DESIGN

STUDY	COMPANY																													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Reliability/Cost Vs. Technology and Application	X																													
Thermal Design						X										X										X				X
Layout Practices (Design Aids)						X		X											X											X
Package Standardization																											X			X
Size Standardization		X																					X							
Catalog Device Performance Margins								X																						
Large Area Hybrid Design						X											X													
Minimize Use of Hermetic Packaging														X																
Cost Vs. Density/Size Tradeoffs																									X					
Next Level Packaging																							X							
Coordinate Design Rules/ Guidelines With ISHM																X														
Standardize Multilayer Interconnection Scheme																	X													
Reliability Vs. Geometry Considerations																							X							
Catalog of Government Used Hybrids																													X	

TABLE 29. STUDIES RECOMMENDED IN THE AREA OF HYBRID MATERIALS AND DEVICES

RECOMMENDED STUDIES	COMPANY 1	2	3 NR	4	5	6	7	8	9	10	11	12	13	14	15 NR	16	17	18 NR	19	20	21	22	23	24	25	26	27	28 NR	29 NR	30
Substrates																														
Thick Film Metallization (Low Cost, Improved Bond Reliability)				X		X				X		X													X	X				
Alumina (Finer Grained, Smoother, Consistent Quality)					X						X	X		X																
Resistor Materials (High Sheet Resistance)																				X										
Thick Film Resistors (Fired on Glass)											X																			
Capacitor Materials (Improved Quality and Density)																							X							
Thin Film Multilayer Resistor/Conductor Networks																X														
Cofired Substrates																	X													
Polyimide Multilayer Substrates														X																
Beryllia Thick Film Substrates							X																							
Devices																														
Burn-in Capability at Chip Level						X																								
Test Capability at Chip Level							X	X																						
Compatibility With Tape Carrier											X																			
Develop Thin Film Active Devices												X																		
Develop Leadless Inverted Devices																										X				
Improve Metallization Adhesion																														X
Develop Moisture Monitoring Device										X			X																	
Packages																														
Improve Design and Producibility					X																	X								
Improve Plating	X																										X			
Develop Nonhermetic Pkgs.																								X						
Other																														
Improved Attachment Adhesives																			X								X			X
Reworkable Contaminant Protective Coatings									X				X																	
Improved Thin Film Etchants																														X
Wire Characterization		X																												
Soldering to Gold Thin Film																														X

TABLE 30. STUDIES RECOMMENDED IN THE AREA OF THIN FILMS

Recommended Project	COMPANY																											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	NR		NR		NR				NR		NR		NR		NR		NR	NR		NR			NR		NR			NR		
Develop Method for Sawing, Separating and Inspecting Ceramic Substrates		X												X																
Develop Totally Automated Thin Film Process (from substrate inspection through visual insp. after resistor trimming)				X																										
Develop High Density Thin Film Multilayer Process						X		X						X		X					X			X						X
Develop Processes to Batch Fabricate Wide Range Sheet Resistivity (10Ω to 5 KΩ/sq) Materials on the Same Substrate				X			X							X																X
Manufacturing Technology for Automated Dynamic Resistor Trimming							X														X									
Conduct Studies to Improve the Adhesion of Thin Film Metals to Ceramic Substrates										X																				
Investigations of Non-Precious Metal Sputtered Materials as Alternates to Gold												X														X				
Evaluate and Define Cleaning and Handling Methods														X																
Establish Materials Compatibility														X																
Evaluate and Define Masking Materials and Methods														X																
Develop Improved Fixturing and Handling Methods																X														
In-process Adhesion and Thickness Measurement Method																X														
Identification of Process Controls & Variables to Permit Combination of Thin and Thick Films																X														

TABLE 30. (cont)

Recommended Project	COMPANY																												
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	NR		NR		NR				NR		NR		NR		NR		NR	NR		NR			NR		NR			NR		
Develop High Stability Resistors & Resistor Passivation Coatings. Study Vacuum Annealing and Stabilization of TaN Resistors to Achieve Low TCR.				X															X			X							X	
Characterize Resistor Geometries/Substrate Materials (to optimize TCR tracking)																						X								
Characterize Gaseous Impurities in Sputtering Environment (effects on metallization properties)																						X								
Evaluate Dry Processing Methods Such as Plasma Photoresist Ashing and Metal Film Etching Using Oxygen and Fluorine Free Radicals, In-Process Substrate Cleaning																X						X								
Develop Processes for Finer Lines/Spacing (0.5 to 1.5 mils) for Conductors & Resistors																						X					X			
Deposition on Large Substrates (10 x 10 inch)																						X								
Investigate Resistor Materials Other Than TaN and NiCr																										X				

TABLE 31. STUDIES RECOMMENDED IN THE AREA OF THICK FILMS

RECOMMENDED STUDIES	Company 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	NR				NR			NR	NR						NR			NR				NR	NR	NR	NR			NR	NR	NR
Characterize available dielectric materials and develop/select materials with low dielectric constants (5-10) even after multiple firings. Study compatibility with fritless gold pastes and substrate warping problem.		X				X	X																							
Apply Thick Film Technology to Microstrip High Frequency Circuits			X																											
Evaluate improved conductors such as non-noble metal conductors and silver conductors for higher conductivity, improved adhesion and lower cost.				X		X	X						X				X												
Develop resistor system compatible with non-noble metal conductors.						X											X												
Develop materials/processes for finer lines/spacings (≈2 mils)				X								X				X													
Develop/investigate improved resistor inks (consistency, stability, TCR, better tracking).				X		X				X			X						X										
Conductor material stress testing.										X																				
Conduct study to improve conductor adhesion and wire bondability.				X							X		X	X						X									
Conduct manufacturing methods study for automatic wire bonding to thick film circuits.											X																			
Develop process for applying and trimming resistors on top dielectric for high density multilayer circuits.							X				X					X														
Develop voltage variable resistor materials												X																		
Increased automation of processes												X																		
Study to increase solder leach resistance of thick film conductors.													X																	

TABLE 31. (cont)

	COMPANY																														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	NR				NR			NR	NR						NR			NR				NR	NR	NR	NR			NR	NR	NR
Full Resistor Characterization (process and design variables/ controls versus performance).																X														
Multilayer, double-sided conductors with interconnections.																X														
Investigate resistor sensitivity to processing													X																	
Cost reduction of multilayer substrates.																	X													
Study effect of particle size distribution on thick-film resistors																					X									
Develop thick-film capacitor pastes having high K values (mixtures of glasses and ferroelectric materials).																										X				
Develop improved organic binders (for conductors) to improve shelf-life and paste stability.																										X				
Develop process for screen printing using Riston photoresist application																										X				
Define resistor/conductor interface effects																											X			
Conduct Manufacturing Technology Program for laser trimming resistors and determining stability of trimmed resistors.																											X			
Develop process technology for manufacturing thick film circuits on beryllia substrates for high power applications							X																							

TABLE 32. STUDIES RECOMMENDED IN THE AREAS OF COMPONENT/SUBSTRATE ATTACHMENT AND INTERCONNECT BONDING

RECOMMENDED STUDIES	Company 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	NR							NR							NR		None	NR		NR					NR			NR	NR	
Manufacturing Technology for the Use of Hermetic Chip Carriers on Large Ceramic Interconnect Brds.			X																											
Manufacturing Technology for Automated (Computer Controlled) Wire Bonding					X		X			X												X								
Conduct Study Comparing TC, TS, & US Bonding (Capibilities, Limitations, Reliability)				X																										X
Ultrasonic Al Ball Bonding						X																								
Improve Bond Characterization Techniques and Define Material Reqmts. & Process Variables Affecting Wire Bonds; Characterize Interconnect Compatibility With Thick Films									X	X						X					X								
Evaluate & Develop Electrical Stress Testing To Check Bond Integrity																X														
Development of Tape Carriers With Alternate Device/ Tape Bumping Methods			X							X	X				X								X			X	X		
Develop Automated Bonding (Sequential) of Tape Chip Carried Devices			X							X																				
Standardize Tape Carried Devices (Standard Size plus Pad Locations)											X	X																		
Manufacturing Technology for Inter-Substrate Wire Bonding													X																	
Soldering to Thick Films													X																	
Ultrasonic Bonding to Thick Films										X																				
Microbonding Techniques for Single Component Attach in an Already High Populated Area														X																
Establish Equipment and Techniques for Automated Wire Pull Testing																			X					X						
Provide Larger Bonding Pads																						X								
Develop Processes and Schedules for Large Diameter Wire Bonding																														X

TABLE 32. (cont)

	Company																												
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Develop Monometallic Systems for More Reliable Bonds						X																								
Identification of Acceptable Epoxies for Substrate and Die Attachment		X								X																				X
Develop and Evaluate Improved Epoxy Adhesives for Better Thermal Stability																			X		X		X			X				X
Evaluate Processes and Materials for the Attachment of Chip Capacitors																			X											
Manufacturing Technology for Alloy Attach (Solder or Alloy Attach of Semiconductors to Substrate)																						X				X				
Low Temperature (<200°C) Substrate Attach																X														
Evaluate Feasibility of Using Components With Preform Material as an Integral Part														X																
Multi-Chip Attachment												X																		
Grounding Under Microwave Substrates													X																	
High Temperature Assembly Processes (>200°C)						X																								

TABLE 33. STUDIES RECOMMENDED IN THE AREA OF PACKAGE SEALING

	COMPANY																												
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Companies Responding "None":	X	X			X		X	X	X	X		X	X		X		X	X	X		X			X				X	X	
RECOMMENDED STUDIES																														
Obtain Data on the Relative Reliability of Different Sealing Methods and Different Solder Alloys			X																											
Develop Equipment for Sealing Flangeless Platform Packages				X																										
Develop Methods to Analyze, Verify/Specify the Sealed Package Ambient						X																								
Investigate Damage to Glass Seals Due to Thermal Screening											X																			
Develop Electron Beam or Laser Welding (Package Materials/Form Factors)														X																
Replace Present Leak Testing Method With Vacuum Deflection Method														X																
Establish Specifications to Control the Quality of Covers, Packages and Preforms																X														X
Evaluate Flow Characteristics on Various Metal Systems																X														
Develop Accurate Method of Measuring Fine Leak Rates for Large Packages																				X										
Develop Low Leak Rate Glass to Metal Seals and Study Effect of Sealing Conditions on Glass Feedthroughs																				X							X			
Develop Sealing Methods & Materials for Large Packages (Flatness/Cleanliness)						X																X	X							
Investigate Use of Ni or Sn Plated Pkgs Instead of Presently Used Gold-plated Pkgs.																						X								
Develop Low Temperature *Substitute for Au/Sn Preform* and Conduct Solder Preform Study																						X				X				
Investigate Effect of Temp. Cycling on Solder Sealed Pkgs.																									X					
Develop Improved Epoxy Materials for Sealing Pkgs.														X																
Studies to Determine Minimum Required Bake-out Time																											X			

TABLE 34. STUDIES RECOMMENDED IN THE AREA OF ELECTRICAL TESTING

	COMPANY																												
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Companies Responding "None":	X	X			X		X	X	X	X	X		X	X	X		X	X	X	X	X			X	X			X		X
RECOMMENDED PROGRAMS																														
Develop Automatic Fault Isolation Procedures			X									X				X							X				X		
Investigate Guard Band Parameter Testing (Instead of Testing at Temp. Extremes) for Both Semiconductors and Hybrids				X																										
Develop Method for 100% AC Testing of Semiconductor Chips Prior to Assembly				X																										
Establish Methods of Multiple Point Probing of Substrate Component Assembly Prior to Packaging						X																								
Develop a Reliable Method of Interconnecting With Hybrids During Temp. Extreme Testing																						X								
Evaluate Value of "Reverse Bias-Conditions A & C"																										X				
Develop Guidelines or Specification Test Requirements																													X	

TABLE 35. STUDIES RECOMMENDED IN THE AREAS OF QUALITY CONTROL/QUALITY ASSURANCE

	COMPANY																														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Companies Responding "None"	X	X			X			X		X	X	X			X		X	X		X	X	X		X	X			X	X	X
What Percentage of Total Hybrid Cost is Due to QC/QA?	33	10	15	20	5	40	20	25	20	40	20	10	-	35	30	20	-	25	18	30	-	5	10	-	-	15	23	-	10	12
RECOMMENDED STUDY PROGRAMS																														
Evaluate Effectiveness of MIL-STD-883B (5004 & 5008) Screen Tests			X																											
Evaluate Reliability Impact of Each of These Screen Tests			X																											
Develop Automatic Visual Inspection Techniques Including Defect Recognition				X			X						X						X											
Develop In-Process Ultrasonic Bond Quality Monitor and Improved Techniques to Characterize Wire Bonds						X			X																					
Develop In-Process Cleanliness Monitor, Simple Low Cost In-Process Moisture Test						X													X											
Develop Quality Test Methods Exclusively for Hybrids														X																
100% Pull Testing for Wire Bonds																X			X											
Evaluate Chemical-Plasma Cleaning Techniques																			X											
Investigate Possibility of Using Smaller Qualification Samples																										X				
Establish Sampling Specification (Similar to MIL-STD-105) for Sampling/Failure Rate Expectancy for Hybrids Only																										X				
Standardize Chip Components (Simple & Complex) for Use In Hybrids																										X				
Evaluate (or Review) Visual Inspection Criteria Vs Reliability																											X			

TABLE 36. STUDIES RECOMMENDED IN THE AREA OF REWORK

	COMPANY																												
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Companies Responding "None":	X							X	X	X		X	X		X	X	X	X		X	X				X			X		X
Is Rework Essential? Yes:	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	X		X	X	X	X		X	X	X	X
No:												X														X				
Is There a Need for Standard Rework Procedures or Guidelines? Yes:			X	X	X	X	X	X						X		X	X	X	X	X		X	X	X	X	X	X			X
No:	X	X							X	X	X	X	X																X	
RECOMMENDED PROGRAM																														
Rework Versus Process and Effect of Reworking Circuits on Long-Term Reliability			X	X	X	X	X																							
Determine Rework Limitations and Establish Rationale				X	X	X	X																				X			
Develop Process/Equipment Reducing Amount of Heat Required											X																			
Suitable Material for Repair of Hermeticity Rejects (Rework of Fine-Leak Pkgs)														X				X												
Establish Methods of Lid Removal/Replacement Including Rework of Welded Pkgs.		X				X													X			X	X	X					X	
Establish Methods of Component Removal and Replacement														X					X			X		X						
Establish Methods of Cleaning Package Being Reworked																			X											
Investigate Use of "Stacked Die" and "Stacked Wire Bonds" to Reduce Repair and Rework Costs																										X				

APPENDIX A

BIBLIOGRAPHY OF REFERENCES

USED IN MANUAL SEARCH

APPENDIX A

REFERENCES FROM MANUAL SEARCH OF CONFERENCE PROCEEDINGS

The following are references from proceedings of five technical conferences held in 1976/1977. The technical articles referenced are keyed to the proceedings references as follows:

(ref. 1) 1977 International Microelectronics Symposium, Oct. 24-26, 1977, Baltimore, MD.

(ref. 2) 13th Electrical/Electronics Insulation Conference, Sept. 25-29, 1977, Chicago, IL.

(ref. 3) U.S. Army Electronics Command Hybrid Microcircuits Symposium, Ft. Monmouth, NJ, June 8-9, 1976.

(ref. 4) 14th IEEE Computer Society International Conference, Feb. 28, 1977, San Francisco, CA.

(ref. 5) 1977 NASA/ISHM Microelectronics Conference, Sept. 20-21, 1977, Marshall Space Flight Center, AL.

(ref. 6) 15th Annual Reliability Physics Symposium, April 12-14, 1977, Las Vegas, NV.

(ref. 7) American Vacuum Society/ISHM, Thick and Thin Films Applications Conference, May 31-June 1, 1977, Los Angeles, CA.

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21. Polymer Thick Film Circuits on Printed Circuit Boards, F. Wayne Martin (ref. 2).

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3. Moisture Related Problems In Hybrids, C. R. Murphy (ref. 1).

4. An Improved Materials System for Maintaining High Resistivity of Electrical Insulation In Humid Environments, C. Harper (ref. 2).

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6. Humidity Threshold Variations For Dendrite Growth on Hybrid Substrates, A. DerMarderosian and C. Murphy (ref. 2).

7. On the Penetration of Gases and Water Vapor Into Packages With Cavities and on Maximum Allowable Leak Rates, D. Stroehle (ref. 2).

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9. Military Requirements for Microelectronics, L. B. Residori (ref. 5).

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TESTS/QUALITY CONTROL

1. Radioisotope Hermetic Test Precision, S. Ruthberg and G. Neff (ref. 1).

2. Hybrid Circuit Qualification at Reduced Cost, T. J. Miles, D. G. Langlais and R. P. Daniel (ref. 1).

3. The Hybrid Microelectronic Process and Quality Control Guide, W. R. Rodrigues de Miranda (ref. 3).

4. Military Quality Control Documents for Hybrid Microcircuits, I. H. Pratt (ref. 3).

5. Marginal Wire Bonds and the Effectiveness of MIL-STD-883 Screens, S. D. Robertson, J. J. Licari and R. L. Buckelew (ref. 1).

6. Strength Tests of 1-Mil Diameter Aluminum Wire Exposed to High Temperature for Various Time Periods, S. C. Piccoli (ref. 1).

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8. Effective Use of Loose Particle Detectors, G. H. Ebel.

9. Sensitivities of Particle Impact Noise Detection, F. Z. Keister and S. V. Caruso (ref. 5).

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1. Total Integration of Microelectronics and Electronic Packaging Design, R. Sandeau (ref. 1).

2. Hybrid and MIC Packaging Design for SHF Satellite Communications Terminals, R. Bigler and F. Farmar (ref. 3).

3. A Novel Hybrid Packaging Scheme for High Component Density Circuits, T. R. Narasimhan (ref. 1).

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5. Computer Aided Design of Hybrid Microcircuits: Four Years of Operating Experience, R. E. Martin, R. R. Shah and M. T. Smith (ref. 1).

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8. Special Problems With Power Hybrids, W. L. Morris (ref. 1).

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1. Influence of Thermal Aging on the Electrical and Mechanical Properties of Conductive Adhesives, J. J. Svitak and A. F. Williams (ref. 1).

2. Mass Changes of Adhesives During Curing, Exposure to Water Vapor, Evacuation and Outgassing, A. W. Czandera, R. Vasofsky and K. K. Czandera (ref. 1).

3. Material Requirements and Process Controls for Epoxy Adhesives Used In Hybrid Microcircuits, J. J. Licari, B. L. Weigand, and K. L. Perkins (ref. 3).

4. Electrically Insulative Adhesives for Hybrid Microelectronic Fabrication, G. W. Brassel (ref. 2).

5. Electrical Properties of Epoxies Used in Hybrid Microelectronics at Low Microwave Frequencies, J. F. Mara and J. E. Sergent (ref. 1).

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1. Insulated Metal Substrates for Power Hybrid ICs, N. Miura, Y. Fuura, A. Kazami, and M. Yamagishi (ref. 1).

2. Metallization of Beryllia Ceramics for Microelectronics Use, J. Bevore (ref. 2).

3. Characteristics of Thick Film Conductors and Resistors on Beryllia Substrates, R. P. Himmel (ref. 1).

4. Pyrolytic Boron Nitride As a Microstrip Substrate Material, C. M. Krowne and T. E. Washburn (ref. 2).

5. Microwave Design Utilization With a New Nonceramic High Dielectric Substrate, W. D. Hutchins (ref. 1).

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1. Reliability Assessment of Hybrid Encapsulants: Fluorinated Network Polymeric Materials and Silicones, A. Christou (ref. 2).

2. Assessment of Silicone Encapsulation Materials: Screening Techniques, A. Christou and W. W. Wilkins (ref. 2).

3. Bubbles....Tiny Bubbles or Pressure and Vacuum Effects on Hybrid Overcoating System, S. A. Bonis (ref. 1).

4. Internal Conformal Coatings for Microcircuits, G. T. Malloy, A. R. Mastro and J. K. Whittington (ref. 2).

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1. Low Dielectric Substrates for MICs at Millimeter Wave Frequencies, J. Reindel (ref. 2).

2. Microwave Design Utilization With a New Nonceramic High Dielectric Substrate, W. D. Hutchins (ref. 1).

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5. Producible Design of MIC Phase Shifters for Phased Array Applications, M. E. Davis (ref. 2).

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8. Millimeter Ferrite Phase Shifters Using Arc Plasma Spray Fabrication Techniques, R. Babbitt, R. A. Stern (ref. 2).

9. Microwave Filters Using Microelectronic Conductor Deposition Technology, W. A. Caton, J. E. Sergent and J. L. Allen (ref. 1).

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1. A New Cleaning Method for Ceramic Microelectronic Substrates, P. G. Creten and D. E. Peters (ref. 1).

2. SEM Modules, J. Fishel (ref. 3).

4. Ruggedized Hybrid Microcircuits, O. P. Layden and F. J. Murdock (ref. 3).

5. Microelectronic/Electronic Packaging Potential, R. F. Sandeau (ref. 5).

6. Investigation of Package Sealing Using Organic Adhesives, K. L. Perkins and J. J. Licari (ref. 5).

7. Cluster Sealing, Raytheon (ref. 5).

8. A Hermetic Sealing Process for Large Irregularly Shaped Hybrid Microci-cuit Enclosures, M. R. Stahler (ref. 5).

9. Techniques for Yield Improvement in Complex Multi-chip Hybrids, S. Polednak and A. Wallace (ref. 1).

APPENDIX B

HYBRID MICROCIRCUITS

COST AND RELIABILITY

QUESTIONNAIRE

HYBRID MICROCIRCUITS COST AND RELIABILITY SURVEY

SECTION I - GENERAL

1. Please estimate the number of hybrid microcircuits (hybrids) of each type produced/purchased per month by your firm and indicate their cost range.

	Number Produced	Cost Range	Number Purchased	Price Range
Thin Film	_____	_____	_____	_____
Thick Film	_____	_____	_____	_____
Co-Fired	_____	_____	_____	_____

2. Of the hybrids produced/purchased per month by your firm, please indicate the number and cost range for each of the following circuit types.

	Number Produced	Cost Range	Number Purchased	Price Range
Digital	_____	_____	_____	_____
Analog	_____	_____	_____	_____
Microwave	_____	_____	_____	_____

3. Of the hybrids produced/purchased per month by your firm, please indicate the number and cost range for those intended for commercial use and for those intended for military use.

	Number Produced	Cost Range	Number Purchased	Price Range
Commercial Use	_____	_____	_____	_____
Military Use	_____	_____	_____	_____

SECTION I - GENERAL (cont)

4. Please indicate the controlling MIL-STD and estimate the number and cost range of the hybrids produced/purchased per month by your firm for military use.

	Number Produced	Cost Range	Number Purchased	Price Range
MIL-STD-883, Class A	_____	_____	_____	_____
MIL-STD-883, Class B	_____	_____	_____	_____
Other (specify)				
	_____	_____	_____	_____

5. To what extent are MIL-STD's followed in the fabrication of hybrids produced/purchased by your firm for commercial use?

6. Of the hybrid microcircuits produced/purchased, please give a range of complexity.

	Produced	Purchased
High: ≥40 components	_____	_____
Medium: >10, <40 components	_____	_____
Low: ≤10 components	_____	_____

SECTION I - GENERAL (cont)

7. In your opinion, what factors make hybrids of comparable complexity more expensive when they are intended for military use than when they are intended for commercial use? Please list factors in order of cost contribution.

8. To what areas of hybrid technology is your firm currently committing discretionary funds (IR&D, burden, etc.) or planning to commit discretionary funds in the immediate future?

9. What specific studies (ranging from basic research to manufacturing technology) do you feel the government should be funding to reduce the cost or improve the reliability of hybrids?

SECTION II - COST FACTORS

1. Please rank the high cost contributors (1, 2, 3, etc.) and from your experience indicate their approximate percentage contribution to total hybrid cost.

	Cost Contrib. Ranking	Percent Contribution
Fabrication Materials (including packages) and Devices	_____	_____
Substrate Fabrication Processes	_____	_____
Assembly and Packaging Processes	_____	_____
Electrical Testing	_____	_____
Quality Control/Quality Assurance	_____	_____
Screen Testing	_____	_____
Rework	_____	_____
Documentation and Customer Interface	_____	_____
Other (indicate) _____	_____	_____

2. If fabrication materials/devices were selected among the high cost contribution, list the highest cost materials/devices and indicate their percentage contribution to this category.

	Percent Contribution
1. _____	_____
2. _____	_____
3. _____	_____

3. If substrate fabrication processes (thin film, thick film, etc.) were selected among the high cost contributors, list the specific processes that are the highest cost contributors and indicate their percentage contribution to this category.

	Percent Contribution
1. _____	_____
2. _____	_____
3. _____	_____

SECTION II - COST FACTORS (cont)

4. If assembly processes (device attachment, interconnect bonding, package sealing, etc.) were selected among the high cost contributors, list the specific processes that are the highest contributors and indicate their percentage contribution to this category.

	% Contribution
1. _____	_____
2. _____	_____
3. _____	_____

5. If electrical testing was selected among the high cost contribution, list the specific tests or related factors that are the highest cost contributors and indicate their % contribution to this category.

	% Contribution
1. _____	_____
2. _____	_____
3. _____	_____

6. If quality control/quality assurance was selected among the high cost contributors, list the specific QC/QA activities that are the highest cost contributors and indicate their percentage contribution to this category.

	% Contribution
1. _____	_____
2. _____	_____
3. _____	_____

7. If screen testing was selected among the high cost contributors, list the main screen tests contributing to the cost and indicate their percentage contribution to this category.

	% Contribution
1. _____	_____
2. _____	_____
3. _____	_____

SECTION II - COST FACTORS (cont)

8. If rework/repair was selected among the high cost contributors, list the elements of rework which contribute most to the cost and indicate their percentage contribution to this category.

	% Contribution
1. _____	_____
2. _____	_____
3. _____	_____

9. If documentation and customer interface was considered a high cost contributor indicate the key areas and their percent contribution to this category.

	% Contribution
1. _____	_____
2. _____	_____
3. _____	_____

10. If an item other than those listed is considered a high cost contributor list the key factors of this item which contribute to cost and their percent contribution to this category.

	% Contribution
1. _____	_____
2. _____	_____
3. _____	_____

HYBRID MICROCIRCUITS COST AND RELIABILITY SURVEY

SECTION III - RELIABILITY

1. What do you consider the key factors affecting the reliability of hybrid microcircuits?

   1.

   2.

   3.

2. Do you feel reliability prediction according to MIL-HDBK 217 is useful for hybrid microcircuits?

   Yes( ) No( )

   Comments?

3. What do you consider the top persistent failure modes in hybrid microcircuits?

   1.

   2.

   3.

SECTION III - RELIABILITY (cont)

4. Should the government sponsor more basic failure mechanism studies?

   Yes( ) No( )

   If yes, list several areas for study.

5. Are your aware of any hybrid problems that are unique to Navy avionics equipment requirements?

   Yes( ) No( )

   If yes, please elaborate.

SECTION IV - HYBRID DESIGN

1. If you have multiple design/production capability, how is type (thick film, thin film, or co-fired) selected for a specific application?

   Customer directed _____
   Management directed _____
   Applications Engineer directed _____
   Layout Designer directed _____
   Determined by analysis _____
   Determined by established guidelines _____

2. Rank the design elements according to their impact on hybrid cost.

   ( ) Power Dissipation
   ( ) Diagnostic Testability
   ( ) Substrate Size
   ( ) Partitioning
   ( ) Resistor Requirements
   ( ) Chip Component Density (per substrate area)
   ( ) Total Component Density (components/substrate area)
   ( ) Next Level Packaging Requirements
   ( ) Number of Conductor Layers
   ( ) Redesign for Production
   ( ) Other _____

3. Are further advances in computer-aided design necessary to reduce hybrid costs?

   What specific advances? _____

   Estimate of cost reduction? _____

SECTION IV - HYBRID DESIGN (cont)

4. What is the maximum number of conductor layers used in your hybrid designs?

   Co-fired _____

   Thin Film _____

   Thick Film _____

   Is there, or will there be, a need for more conductor layers/

   Yes( ) No( ) How many?_____

5. What minimum line widths and spacings do you use in your designs?

	Line Width	Line Spacing
Thin Film	_____	_____
Thick Film	_____	_____
Co-fired	_____	_____

   What minimum line widths and spacings do you feel there is, or will be a need for?

6. Do you feel the government should sponsor programs to standardize on design guidelines for industry?

   Yes( ) No( )

7. What studies, if any, do you feel the government should fund in the area of hybrid design?

HYBRID MICROCIRCUITS COST AND RELIABILITY SURVEY

SECTION V - MATERIALS/DEVICES

1. What devices consistently present problems and require rework?

2. What materials consistently present problems?
Please rank in order of frequency.

Substrates	_____
Thick Film Pastes	_____
Thin Film Metallization	_____
Packages	_____
Sealing Preforms	_____
Epoxy Adhesives	_____
Solder	_____
Wire	_____
Other (indicate)_____	_____

SECTION V - MATERIALS/DEVICES

3. Please suggest any programs in the hybrid materials or devices area that you feel should be performed and indicate whether they would significantly improve reliability, reduce cost, or are needed to meet future system requirements.

Recommended Programs	Improve Reliability	Reduce Cost	Meet Future System Reqmts.
1.	_____	_____	_____
2.	_____	_____	_____
3.	_____	_____	_____

4. Do you feel it would be desirable to have a set of standard specifications and tests for receiving inspection of all hybrid materials and devices to be used throughout industry?

   Comments?

SECTION VI - SUBSTRATE FABRICATION PROCESSES

A. THIN FILMS

1. Are the state-of-the-art substrate materials adequate in meeting your design requirements?

   If not, what is needed?

2. Are the state-of-the-art thin film conductor metallizations adequate in meeting your design requirements?

   If not, what is needed?

3. Do the current thin film resistors meet all your design requirements?

   If not, what is required?

4. Do you feel that passivation of thin film resistors is beneficial to enhancing stability?

   Are new or improved passivation materials or processes needed?

5. Do you feel the government should fund programs to develop thin film multilayer processes?

6. Is there a need for standard or improved test methods for thin film resistor characterization?

SECTION VI - SUBSTRATE FABRICATION PROCESSES (cont)

A. THIN FILMS (cont)

7. Please rank the following thin film process steps in the following three categories.

	Throughput Per Labor Hour	Yield	Worth Automating
a. Substrate inspection	_____	_____	_____
b. Substrate cleaning	_____	_____	_____
c. Deposition	_____	_____	_____
d. Plating	_____	_____	_____
e. Delineation	_____	_____	_____
f. Annealing	_____	_____	_____
g. Temp. Stabilization	_____	_____	_____
h. Resistor trimming	_____	_____	_____
i. In-process testing	_____	_____	_____
j. Visual inspection	_____	_____	_____
k. Other(s):_____	_____	_____	_____

8. What programs/studies (in thin films) would you recommend?

Indicate: R for Fundamental Research
D for Development
MT for Manufacturing Technology

SECTION VI - SUBSTRATE FABRICATION PROCESSES (cont)

B. Thick Films

1. Are the state-of-the-art substrate materials adequate in meeting your design requirements?

   If not, what is needed?

2. Are the state-of-the-art thick film conductor metallizations adequate in meeting your design requirements?

   If not, what is needed?

3. Do the current thick film resistors meet all your design requirements?

   If not, what is required?

4. Do you feel that passivation of thick film resistors is beneficial to enhancing stability?

   Are new or improved passivation materials or processes needed?

5. Do the current thick film dielectrics meet all your design requirements?

   If not, what is required?

SECTION VI - SUBSTRATE FABRICATION PROCESSES (cont)

B. Thick Film (cont)

6. Is there a need for standard or improved test methods for thick film resistor characterization?

7. Please rank the following thick film process steps in the following three categories.

	Throughput Per Labor Hour	Yield	Worth Automating
a. Substrate inspection			
b. Substrate cleaning			
c. Screen, dry, fire conductors			
d. Screen, dry, fire resistors			
e. Screen, dry, fire dielectrics			
f. Resistor Trimming			
g. In-process testing			
h. Visual inspection			
i. Other(s) _____			

8. What programs/studies in thick films would you recommend?

Indicate: R for Fundamental Research
D for Development
MT for Manufacturing Technology

SECTION VII - ASSEMBLY PROCESSES

A. COMPONENT/SUBSTRATE ATTACHMENT AND INTERCONNECT BONDING

1. If you use alloy attachment, what problems have you encountered (briefly)?

2. If you use epoxy attachment, what problems have you encountered (briefly)?

3. If epoxies are used, how are they applied? Please rank in order of usage.

   By hand using a probe ( )

   By syring, hand actuated ( )

   By syring, mechanically actuated ( )

   By stamping ( )

   By screening ( )

   Other _____ ( )

4. If epoxies are used, how do you position components?

   Vacuum probe/tweezers and hand alignment ( )

   Die collet and mechanical positioner ( )

   Split image and mirror system ( )

   Totally mechanical ( )

   Other _____ ( )

5. Is there a need for further investigation or development of completely automated epoxy dispensing and component positioning methods?

SECTION VII - ASSEMBLY PROCESSES (cont)

A. Component/Substrate Attachment & Interconnect Bonding (cont)

6. Which interconnection technology do you consider the most cost effective in each of the listed applications?

	Military High Reliability	Commercial
Chip and Wire	_____	_____
Flip-chip	_____	_____
Beam Lead	_____	_____
Tape Carrier	_____	_____
Leadless Inverted Device	_____	_____
Other_____	_____	_____

7. Please rank the wire and/or ribbon bonding processes used by your firm in order of usage and indicate present and future status of automation.

	Use Ranking	Automation Present		Future	
		Yes	No	Yes	No
Ultrasonic	( )	( )	( )	( )	( )
Thermocompression	( )	( )	( )	( )	( )
Thermosonic	( )	( )	( )	( )	( )
Other_____	( )	( )	( )	( )	( )

8. Do you feel that the tape carrier approach to automated bonding will substantially benefit the assembly of military hybrids?

Please indicate reasons, pro or con.

SECTION VII - ASSEMBLY PROCESSES (cont)

A. Component/Substrate Attachment and Interconnect Bonding (cont)

9. Is there a need for improved or new interconnect technologies?

10. What programs/or studies in the areas or component attachment, substrate attachment or interconnect bonding would you recommend?

Indicate: R for Fundamental Research
D for Development
MT for Manufacturing Technology

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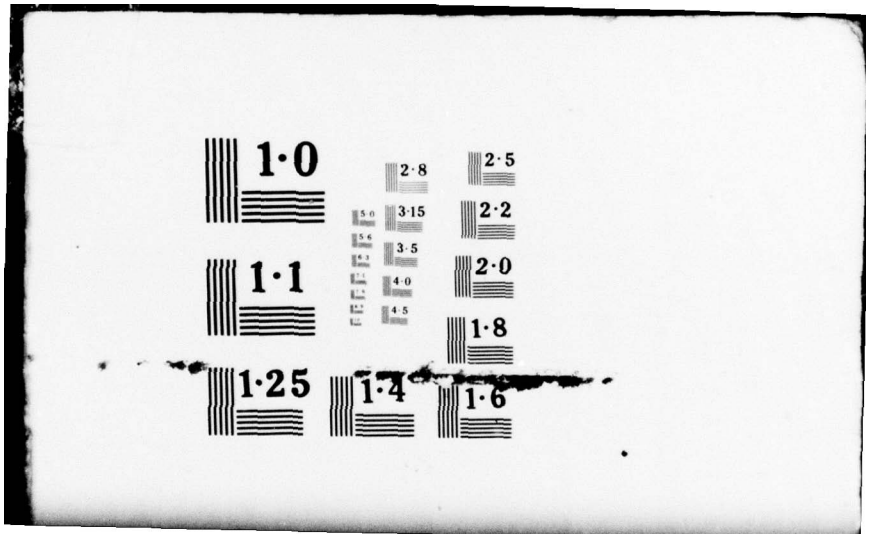
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SECTION VII - ASSEMBLY PROCESSES (cont)

B. PACKAGING

1. Please check the package sealing methods used by your firm and approximate yield at first seal.

	Used	Approx. Yield
Welding (specify type)_____	( )	_____
Resistance Seam	( )	_____
Continuous Belt Furnace	( )	_____
GTI-Type (Dix)	( )	_____
Heated Stage	( )	_____
Manual Soldering	( )	_____
Epoxy	( )	_____
Other (Specify) _____	( )	_____

2. Please rank the types of packages, lids and materials used by your firm in order of usage.

Packages:
- Uniwall ( )
- Modular Sidewall ( )
- Dual-in-line ( )
- Vertical Sidewall ( )
- Butterfly ( )
- Dihedral ( )
- Plug-in (Platform) ( )
- Other (specify)_____ ( )

Lids:
- Flat ( )
- Step ( )
- Domed ( )

Materials:
- Gold Plated Kovar ( )
- Gold Plated Alloy 4-2 ( )
- Other (specify)_____ ( )
- 50 Microinch Au Plating ( )
- 100 " Au Plating ( )
- 150 " Au Plating ( )
- Other _____ ( )

SECTION VII - ASSEMBLY PROCESSES (cont)

B. Packaging (cont)

3. Please indicate the bake-out schedule (time/temperature/vacuum) which you use for hybrid microcircuits?

4. Please rank the methods you use for leak testing according to usage:

Gross:	.MIL-STD-883A, Method C_1	( )
	Method C_2	( )
	Method D	( )
	Method E	( )
	Other (specify) _____	( )
Fine:	MIL-STD-883A, Method A_1	( )
	Method A_2	( )
	Method A_3	( )
	Method B	( )

5. Indicate leak rate criterion used for acceptance of sealed packages. State whether helium or air equivalent?

	atm. cc/sec
Packages - volume ≤0.1 cc	_____
Packages - volume >0.1 cc <10 cc	_____

6. From your experience in sealing hybrid packages, what materials procedure and criteria would you recommend as a standard?

Package Type (case, lid and material)	_____
Sealing Method	_____
Presealing Procedure (e.g., abrasion of seal area)	_____
Bake-out Parameters	_____
Gross Leak Test(s)	_____
Fine Leak Test(s)	_____
Fine Leak Acceptance Criterion (indicate whether helium or air equivalent) _____	_____

SECTION VII - ASSEMBLY PROCESSES (cont)

B. Packaging (cont)

7. What specific areas of package sealing have given you problems and what studies do you feel should be undertaken?

C. General

Please rank the following assembly process steps in the following three categories:

	Throughput per Labor Hour	Yield	Worth Automating
Substrate attachment			
Die/component attachment			
Interconnect Bonding			
Total cleaning processes			
In-Process Testing			
Inspection			
Marking/Serialization			
Sealing			
Hermetic Testing			
Other_____			

SECTION VIII - ELECTRICAL TESTING

1. Do you purchase semiconductor chips:

   Tested by manufacturer ( )

   Tested in-house prior to hybrid assembly ( )

   Tested by a third party ( )

2. Do you have the semiconductor chips:

   a. Tested to the manufacturer's d.c. probe test only ( )

   b. Tested to a.c. parameters ( )

   c. Lot sample tested ( )

   d. Tested at high temperature ( ) ( )°C

   e. Tested at low temperature ( ) ( )°C

   f. Tested to special parameter requirements ( )

   Which of the above do you consider best from a cost/ reliability tradeoff standpoint?

3. Do you have passive components (resistors and capacitors):

   a. Tested to manufacturer's specifications only ( )

   b. Lot sample tested ( )

   c. Tested at temperature extremes ( )

   d. Tested to special requirements ( )

   Which of the above do you consider best from a cost/ reliability trade-off standpoint?

SECTION VIII - ELECTRICAL TESTING (cont)

4. Do you subject the substrates to:

   a. Resistor test and trim only ( )

   b. 100 percent conductor continuity ( )

   c. Conductor isolation ( )

   Which of the above do you consider best from a cost/reliability trade-off standpoint?

5. Indicate points in the process at which you perform electrical testing and give approximate yields.

	Test	Yield
a. Prior to substrate installation in package	_____	_____
b. Preseal	_____	_____
c. Post-seal	_____	_____
d. After each environmental screen; i.e., temperature cycling, constant acceleration, mechanical shock, etc.	_____	_____
e. Pre-burn-in	_____	_____
f. Post burn-in	_____	_____
g. Final acceptance	_____	_____

   Which of the above do you consider most effective from a cost/reliability standpoint?

6. Approximately what percentage of the hybrids that you manufacture are subjected to delta parameter testing for the burn-in screen test?

   Comments?

SECTION VIII - ELECTRICAL TESTING (cont)

7. Approximately what percentage of the hybrids that you manufacture must meet a percent defective allowable (PDA) requirement?

8. Do you utilize automatic test for

   Analog circuits ( )

   Digital circuits ( )

9. Do you have fault diagnostic capability or do you simply throw away circuits that do not pass?

10. If you have automatic fault diagnostic capability, what is your estimate of the percent effectiveness of that capability?

11. If you use manual fault diagnosis, what is your estimate of the percent effectiveness of that capability?

12. What government-funded programs would you recommend in the area of electrical testing to reduce costs or improve reliability?

SECTION IX - QUALITY CONTROL/QUALITY ASSURANCE

1. Approximately what percentage of the total cost of a hybrid is due to quality control/quality assurance activities? _____%.

   Rank Quality Assurance/Quality Control functions in order of cost and effectiveness (1 = highest cost/most effective).

	Cost Ranking	Effectiveness Ranking
Adherence to MIL-M-38510	_____	_____
Equipment calibration	_____	_____
Equipment certification	_____	_____
Operator training and certification	_____	_____
Materials review	_____	_____
Incoming inspection	_____	_____
Product inspection/acceptance	_____	_____
Process verification	_____	_____
Qualification testing	_____	_____
In-process monitoring	_____	_____
Specifications and operator instructions and procedures	_____	_____
Customer interfacing	_____	_____
Other _____	_____	_____

2. What recommendations would you propose to streamline or reduce the overall cost of Quality Control/Quality Assurance activities?

3. In those cases when MIL-M-38510 is a controlling document, what deviations (if any) are usually taken?

4. Are there any specific study programs that should be performed in the area of quality control/quality assurance?

SECTION X - SCREEN TESTING

1. Do you perform screen testing on devices prior to assembly in a hybrid?

	Yes	No
IC's	( )	( )
Transistors	( )	( )
Capacitors	( )	( )
Resistors	( )	( )

What type of screens?

Visual _____
Electrical_____
Burn-in _____

2. Please indicate which of the MIL-STD-883 screens you perform and rank them according to your opinion of their effectiveness on long-term reliability.

	Perform	Rank
Visual Method 2010	_____	_____
Visual Method 2017	_____	_____
Stabilization Bake Method 1008	_____	_____
Thermal Shock Method 1011	_____	_____
Temperature Cycling Method 1010	_____	_____
Mechanical Shock Method 2002	_____	_____
Constant Acceleration Method 2001	_____	_____
Seal Method 1014	_____	_____
Fine	_____	_____
Gross	_____	_____
Burn-in Method 1015 (240 hrs at 125°C)	_____	_____
Burn-in Method 1015 (160 hrs at 125°C	_____	_____
Reverse Bias Method 1015 (72 hrs at 150°C)	_____	_____
Radiographic Method 2012	_____	_____
External Visual Method 2009	_____	_____
PIND Test Method 2020	_____	_____
Moisture Method 5008	_____	_____

SECTION X - SCREEN TESTING (cont)

3. What percent of hybrids fail the imposed screens?

   Analog _____

   Digital _____

   Combined _____

4. Do you consider the environmental screens of MIL-STD-883 and the required test conditions for Class A or B to be

	Class A	Class B
Loose	( )	( )
Moderate	( )	( )
Harsh	( )	( )

5. Do you consider Method 5008 of MIL-STD-883A for moisture limitation realistic and/or cost effective? Yes ( ) No ( )

   Comments: _____

6. Do you believe DoD is obtaining a proper return for its screening dollar when considering cost of ownership of equipment containing hybrid microcircuits?

   Good Return _____ Poor Return _____

   Comments:

7. Would you recommend the addition of any new screen tests or the elimination of any existing screen tests?

   Comments?

SECTION XI - REWORK

1. Indicate whether you allow rework for the following and rank according to frequency of rework (highest rework frequency = 1).

	Military High Rel. Yes	Military High Rel. Frequency	Commercial Yes	Commercial Frequency
a. Passive substrate	___	_____	___	_____
b. Active device replacement	___	_____	___	_____
c. Passive device replacement	___	_____	___	_____
d. Beam lead replacement	___	_____	___	_____
e. Wire bond to device	___	_____	___	_____
f. Package and lid	___	_____	___	_____
g. Package seal	___	_____	___	_____
h. After seal	___	_____	___	_____
i. Other _____	___	_____	___	_____

2. Which of the above are being performed in accordance with specifications?
   What specifications?

   Are the specifications adequate?

3. Is the amount or number of reworks limited by specification? Yes( ) No( )
   What specifications?
   Is there sufficient engineering on experimental data to justify the number of reworks allowed? Yes ( ) No ( )

4. What is the rationale behind the rework limitation?

   Process limitation _____

   Device limitation _____

   Process compatibility _____

   Process sequence _____

   Customer specifications _____

   Economic _____

   Other _____

SECTION XI - REWORK (cont)

5. Do you feel rework is essential in meeting cost and schedule requirements?

6. Do rework processes differ from original or first through process?

7. Is the amount of rework monitored for process control corrective action?

8. Is there a relationship between allowed rework and circuit density?

9. Is a throw-away concept feasible with hybrids?

   If so, what is the criteria?

10. Is there a need for standard rework procedures or guidelines that can be used throughout industry?

11. What government sponsored programs, if any, would you recommend in the area of rework?

    Indicate: R for Research
    D for Development
    MT for Manufacturing Technology